Announcing the Final Examination of Majd Batarseh for the degree of Doctor of Philosophy

Time & Location: December 9, 2009 at 10:00 AM in HEC 437
Title: Digital Pulse Width Modulator Techniques for DC-DC Converters

Recent research activities focused on improving the steady state as well as the dynamic behavior of DC-DC converters for proper system performance by proposing different design methods and control approaches with growing tendency to using digital implementation over analog practices. Because of the rapid advancement in Integrated Circuits (ICs) and microprocessor industry, digital control grew in popularity among Pulse Width Modulator (PWM) converters and is taking over analog techniques due to their fast speed microprocessors, flexibility and immunity to noise and environmental variations. Furthermore, increased interest in Field Programmable Gate Arrays (FPGA) makes it a convenient design platform for digitally controlled converters.

The objective of this research is to propose new digital control schemes aiming to improve the steady state and transient responses of FPGA-based digitally controlled DC-DC converters for various computer and telecommunication applications. The improvements aim at achieving tighter DC output regulation at steady state with minimum power consumption and high efficiency as well as shorter settling time with optimal over- and undershoot during transients. The main task is to revisit the conventional Digital Pulse Width Modulator (DPWM) and modify in order to achieve:
1. Tight regulation at steady state by proposing high resolution DPWM architecture based on Digital Clock Management resources available on FPGA boards. The proposed architecture Window-Masked Segmented Digital Clock Manager-FPGA based Digital Pulse Width Modulator Technique, is designed to achieve high resolution operating at high switching frequencies with minimum power consumption.
2. Enhanced dynamic response by applying dynamic shift to the basic saw-tooth DPWM signal, in order to benefit from the best linearity and simplest architecture offered by the conventional counter-comparator DPWM. This proposed control scheme helps the compensator reach the steady state value faster and thus achieves better transient behavior.

Major: Electrical Engineering

Educational Career:
Bachelor's of Electrical Engineering, BS, 2004, University of Jordan
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Committee in Charge:
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Dr. Chris Iannello, National Aeronautics and Space Administration, NASA

Approved for distribution by Dr. Issa Batarseh, Committee Chair, on November 23, 2009.

The public is welcome to attend.