Announcing the Final Examination of Sumedha Kodipyaka for the degree of Master of Science

Time & Location: November 30, 2009 at 11:00 AM in HEC 438
Title: Reconfigurable Architecture for H.264/AVC Variable Block Size Motion Estimation Using Motion Activity and Adaptive Search Range

Motion Estimation (ME) technique plays a key role in the video coding systems to achieve high compression ratios by removing temporal redundancies among video frames. Especially in the newest H.264/AVC video coding standard, ME engine demands large amount of computational capabilities due to its support for wide range of different block sizes for a given macroblock in order to increase accuracy in finding best matching block in the previous frames.

We propose scalable architecture for H.264/AVC Variable Block Size (VBS) Motion Estimation with adaptive computing capability to support various search ranges, input video resolutions, and frame rates. Hardware architecture of the proposed ME consists of scalable Sum of Absolute Difference (SAD) arrays which can perform Full Search Block Matching Algorithm (FSBMA) for smaller 4x4 blocks. It is also shown that by predicting motion activity and adaptively adjusting the Search Range (SR) on the reconfigurable hardware platform, the computational cost of ME required for inter-frame encoding in H.264/AVC video coding standard can be reduced significantly with only small degradation in PSNR (≤0.1dB).

Dynamic Partial Reconfiguration is a unique feature of Field Programmable Gate Arrays (FPGAs) that makes best use of hardware resources and power by allowing adaptive algorithm to be implemented during run-time. We exploit this feature of FPGA to implement the proposed reconfigurable architecture of ME and maximize the architectural benefits through prediction of motion activities in the video sequences and adaptation of SR during run-time. The implemented ME architecture can support real time applications at a maximum frequency of 90MHz with multiple reconfigurable regions. By increasing the number of active partial reconfigurable modules from one to four, data reuse in the proposed scalable ME architecture can be increased 4 times, resulting in reduction of the required frame memory bandwidth.

Major: Electrical Engineering

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Bachelor's of Electronics and Communication Engineering, BS, 2007, Osmania University, Hyderabad, India

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Approved for distribution by Dr. Joohheung Lee, Committee Chair, on November 13, 2009.

The public is welcome to attend.