Strain engineering, especially strained Si/SiGe is widely adopted in modern high performance semiconductor devices. In this thesis, three novel structures are proposed for N-type and P-type trench power MOSFET as well as LDMOS to increase mobility utilizing strained Si/SiGe. A set of fabrication process highly compatible with conventional Si technology is also developed.

The proposed process flow is simulated and the generated device is inspected and optimized using Synopsis TCAD tools. The result shows electron and hole mobility are enhanced by up to 20% and 50% respectively. The specific conduction resistance is reduced by 10% for NMOSFET and 20% for PMOSFET while maintaining other device performances.

Educational Career:
Bachelor's of Electrical Engineering, BS, 2005, Shanghai Jiaotong University

Committee in Charge:
John Shen, Chair, EECS
J.S Yuan, EECS
Thomas Wu, EECS
Linan An, Mechanical Engineering

Approved for distribution by John Shen, Committee Chair, on August 1, 2010.

The public is welcome to attend.