Electrostatic discharge (ESD) is defined as the transfer of charge between bodies at different potentials. The electrostatic discharge induced integrated circuit damages occur throughout the whole life of a product from the manufacturing, testing, shipping, handing, to end user operating stages. This is particularly true as microelectronics technology continues shrink to nano-metric dimensions. The ESD related failures is a major IC reliability concern and results in a loss of millions dollars to the semiconductor industry each year. Several ESD stress models and test methods have been developed to reproduce the real world ESD discharge events and quantify the sensitivity of ESD protection structures. The basic ESD models are: Human body model (HBM), Machine model (MM), and Charged device model (CDM). To avoid or reduce the IC failure due to ESD, the on-chip ESD protection structures and schemes have been implemented to discharge ESD current and clamp overstress voltage under different ESD stress events. Because of its simple structure and good performance, the junction diode is widely used in on-chip ESD protection applications. This is particularly true for ESD protection of low-voltage ICs where a relatively low trigger voltage for the ESD protection device is required. Two types of diodes with different anode/cathode isolation technologies will be investigated for their ESD performance: one with a LOCOS (Local Oxidation of Silicon) oxide isolation called the LOCOS-bound diode, the other with a polysilicon gate isolation called the poly-bound diode. We first examine the ESD performance of the LOCOS-bound diode. The effects of different diode geometries, metal connection patterns, dimensions and junction configurations on the ESD robustness and parasitic capacitance are investigated experimentally. Then, the current carrying and voltage clamping capabilities of LOCOS- and poly-bound diode diodes are compared and investigated based on both TCAD simulation and experimental results. Comparison of these capabilities leads to the conclusion that the poly-bound diode is more suited for ESD protection application due to its higher performance. The effects of poly-bound diode's design parameters, including the diode width, cathode length, finger number, poly-gate length, terminal connection and metal topology, on the ESD robustness are studied. Two figures of merits are developed to better assess the effects of different parameters on poly-bound diode's overall ESD performance. As latest generation package styles such as mBGAs, SOTs, SC70s, & CSPs are going to the mm-range dimensions, they are often effectively too small for people to handle with fingers. The recent industry data indicates the CDM ESD event becomes increasingly important in today's manufacturing environment and packaging technology. This event generates highly destructive pulses with a very short rise time and very small duration. The overshoot voltage and turn-on time are two key considerations for designing the CDM ESD protection devices.Transient behaviors of poly-bound diode subject to pulses generated by the VFTLP tester are characterized for fast ESD events. The effects of changing devices' dimension parameters on the overshoot voltage and turn-on time are studied. The correlation between the diode failure and poly-gate configuration under the VFTLP stress is also investigated.

Major: Electrical Engineering

Educational Career:
Bachelor's of Electrical Engineering, BS, 2003, University of Electronic Science and Technology of China
Master's of Electrical Engineering, MS, 2007, University of Central Florida

Committee in Charge:
Dr. Jin J. Liou, Chair, Electrical Engineering
Dr. James E. Vinson, Intersil Corporation
Dr. Jiann S. Yuan, Electrical Engineering
Dr. Kalpathy B. Sundaram, Electrical Engineering
Approved for distribution by Dr. Juin J. Liou, Committee Chair, on August 11, 2010.

The public is welcome to attend.