Electrostatic Discharge (ESD) phenomenon happens everywhere in our daily life. And it can occurs through the whole lifespan of an Integrated Circuit (IC), from the early wafer fabrication process, extending to assembly operation, and finally ending at the user's site. It has been reported that up to 35% of total IC field failures are ESD-induced, with estimated annual costs to the IC industry running to several billion dollars. The most straightforward way to avoid the ICs suffering the threatening of ESD damages is to develop on-chip ESD protection circuits which can afford a robust, low-impedance bypassing path to divert the ESD pulse to the ground.

There are three different types of popular ESD protection devices widely used in the industry, and they are diodes or diodes string, Grounded-gate NMOS (GGNMOS) and Silicon Controlled Rectifier (SCR). Among these different protection solutions, SCR devices have the highest ESD current conduction capability due to the conductivity modulation effect. But SCR devices also have several shortcomings such as the higher triggering point, the lower clamping voltage etc, which will become obstacle for SCR to be widely used as an ESD protection solutions in most of the industry IC products. At first, in some applications with pin voltage goes below ground or above the VDD, dual directional protection between each two pins are desired. The traditional dual-directional SCR structures will consume a larger silicon area or lead to big leakage current issue due to the happening of punch-through effect. A new and improved SCR structure for low-triggering ESD applications has been proposed in this dissertation and successfully realized in a BiCMOS process. Such a structure possesses the desirable characteristics of a dual-polarity conduction, low trigger voltage, small leakage current, large failing current, adjustable holding voltage, and compact size.

Another issue with SCR devices is its deep snapback or lower holding voltage, which normally will lead to the latch-up happen. To make SCR devices immunity with latch-up, it is required to elevate its holding voltage to be larger than the circuits operational voltage, which can be several tens volts in modern power electronic circuits. Two possible solutions have been proposed to resolve this issue. One solution is accomplished by using a segmented emitter topology based on the concept that the holding voltage can be increased by reducing the emitter injection efficiency. Experimental data show that the new SCR can posses a holding voltage that is larger than 40V and a failure current \( I_{t2} \) that is higher than 28mA/um. The other solution is accomplished by stacking several low triggering voltage high holding voltage SCR cells together. The TLP measurement results show that this novel SCR stacking structure has an extremely high holding voltage, very small snapback, and acceptable failure current. The High Holding Voltage Figure of Merit (HHVFOM) has been proposed to be a criterion for different high holding voltage solutions. The HHVFOM comparison of our proposed structures and the existing high holding voltage solutions also show the advantages of our work.

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The public is welcome to attend.