Copper (Cu) through-silicon via (TSV) is an essential structural and functional element in 3D integrated circuits (3D ICs), which offers substantial improvements in integration density, form factor, device performance, and power efficiency. However, TSVs are prone to thermo-mechanical reliability issues due to the large mismatch of CTE between Cu and Si, as they are exposed to multiple thermal cycles during fabrication, test, and operation. Among the reliability issues for TSVs, via extrusion is an important one, which can result in degradation and failure of the device. Furthermore, there is a wide spread in the values of via extrusion, controlling of which remains an important issue, as the reliability of a 3D IC will be determined by a very small fraction of TSVs with the highest extrusion heights.

This work proposes the application of a metallic cap layer as a novel and promising solution to TSV extrusion variation and investigates its effects on TSV extrusion behavior and the underlying mechanisms with the ultimate goal of assessing and addressing this reliability risk for 3D integration technology. Experimental results first establish the application of different metallic cap layers on TSV samples and demonstrate that Tantalum is an effective cap material to control the magnitude of extrusion, and more importantly, the range of extrusion. In addition, the effect of pitch size and microstructure on extrusion height and morphology are statistically investigated. The mechanisms of extrusion and their correlation to the extrusion morphology and the Cu microstructural characteristics are examined in order to trace the root cause(s) of the high statistical spread in TSV extrusion and the effect of cap layer in controlling the extrusion.

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Approved for distribution by Tengfei Jiang, Committee Chair, on June 16, 2020.

The public is welcome to attend.