Announcing the Final Examination of Jie Lin for the degree of Doctor of Philosophy

Time & Location: March 4, 2020 at 1:30 PM in Research 1 103
Title: Ultra-low Power Circuits and Architectures for Neuromorphic Computing Accelerators with Emerging TFETs and ReRAMs

To design the ultra-low voltage and ultra-low power analog-to-digital converters (ADCs) for the neuromorphic computing systems, we explore advantages of tunnel field-effect transistor (TFET) analog-to-digital converters (ADCs) on energy efficiency and temperature stability. A fully-differential SAR ADC is designed using 20 nm TFET technology with doubled input swing and controlled comparator input common-mode voltage.

To further increase the resolution of the ADC, we design an energy-efficient 12-bit noise shaping (NS) successive-approximation register (SAR) ADC. The 2nd-order noise shaping architecture with multiple feed-forward paths is adopted and analyzed to optimize system design parameters. By utilizing tunnel field-effect transistors (TFETs), the $\Delta$Sigma SAR is realized under an ultra-low supply voltage VDD with high energy efficiency.

The stochastic neuron is a key for event-based probabilistic neural networks. We propose a stochastic neuron using a metal-oxide resistive random-access memory (ReRAM). The ReRAM's conducting filament with built-in stochasticity is used to mimic the neuron's membrane capacitor, which temporally integrates input spikes. A capacitor-less neuron circuit is designed, laid out, and simulated. The output spiking train of the neuron obeys the Poisson distribution.

We address the scaling and power bottlenecks of neuromorphic architecture by utilizing a single one-transistor-one-ReRAM (1T1R) cell to emulate the neuron. We show that the ReRAM-based neurons can be integrated within the synaptic crossbar to build extremely dense Process Element (PE)-spiking neural network in-memory array-with high throughput. We provide microarchitecture and circuit designs to enable the deep spiking neural network computing in memory with an insignificant area overhead.

Major: Electrical Engineering

Educational Career:
Bachelor's of Electronic Information Engineering, BS, 2006, University of Electronic Science and Technology of China
Master's of Circuit and System, MS, 2009, University of Electronic Science and Technology of China

Committee in Charge:
Jiann—Shiun Yuan, Chair, Electrical and Computer Engineering
Kalpathy B. Sundaram, Electrical and Computing Engineering
Mingjie Lin, Electrical and Computer Engineering
Rickard Ewetz, Electrical and Computing Engineering
Zixi (Jack) Cheng, Burnett School of Biomedical Sciences

Approved for distribution by Jiann-Shiun Yuan, Committee Chair, on October 17, 2019.

The public is welcome to attend.