In this work the Electrostatic Discharge (ESD) behavior of GaN on Si power devices is investigated using on-wafer transmission line pulse (TLP) and very fast transmission line pulse (VFTLP). TLP testing results are formulated into I-V plots that are used to uncover underlying device mechanisms by analyzing trigger voltage and holding voltage extracted from the I-V curves. Using this information from multiple devices, several underlying mechanisms and anomalies were observed. Experimentation is then followed up by TCAD simulations.

The devices chosen for this investigation will very in critical device lengths to help uncover the effects of device geometry on ESD robustness. These dimensions are $L_{sg}$, $L_g$, and $L_{gd}$. Device lengths are observed to distinctly influence device triggering under TLP and VFTLP as a result of electric field dependence. TLP testing resulted in much lower triggering voltages due to non-uniform self-heating effects than the more uniform VFTLP which reaches a higher critical electric field. Through continued testing holding voltage appears to be independent of the electric field in the channel under TLP stress. But under VFTLP it is shown that more surface traps are activated leading to increased resistance in the surface and as such an increase in holding voltage.

Further investigation will then be conducted by changing the gate bias between floating and off state to evaluate the effect on surface traps. When comparing floating and off gate it is observed that triggering and holding voltage is influenced by gate bias under both TLP and VFTLP stress. Under TLP triggering is shown to have a monotonic increase under off gate bias shows while in contrast VFTLP actually decreases due to piezoelectric effects induced in the buffer. Furthermore under TLP holding is believed to be related to surface traps induced by the off gate's increased surface electric field.

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The public is welcome to attend.