The extensive use of Integrated Circuits (ICs) means complex working conditions for these tiny chips. To guarantee the ICs could work properly in various environments, some special protection strategies are required to improve the reliability of system. From all the possible reliability issues, the electrostatics discharge (ESD) might be the most common one. The peak current of electrostatics can be as high as tens of amperes and the peak voltage can be over thousand voltages. In contrast, the size of semiconductor device fabricated is continuing to scale down, making it even more vulnerable to high level overstress and current surge induced by ESD event. To protect the on-chip semiconductor from damage, some extra clamp cells are put together to consist a network. The network can redirect the superfluous current through the ESD network and clamp the voltage to a low level.

In this dissertation, one design concept is introduced that uses the combination of some basic ESD devices to meet different requirements first, and then tries to establish parasitic current path among these devices to further increase the current handling capability.

Some design cases are addressed to demonstrate this design concept is valid and efficient: 1. A combination of silicon-controlled-rectifier (SCR) and diode cluster is implemented to resolve the overshoot issue under fast ESD event. 2. A new SCR structure is introduced, which can be used as a padding device to increase the clamping voltage without affecting other parameters. 3. A controllable SCR clamp structure is introduced, which has high current handling capability and can be controlled. All these structures and topologies introduced in this dissertation are compatible with most of the frequently utilized process.

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The public is welcome to attend.