Electrostatic discharge (ESD) is an event that charges suddenly transfer between two objects at different static potentials. It is estimated that about 35% of all damaged microchips are ESD related, resulting in more than 84 billion dollars lost profits per year. The main damage mechanisms of ESD failure include junction thermal failure, oxide rupture, charge injection and metal burnout. Although the SPICE model is accurate and efficient for circuit simulations in most design cases, devices under ESD events operate in abnormal status. Under ESD stresses, semiconductor devices are pushed into high current and high voltage stages, even to irreversible thermal failure. And SPICE model is not able to cover the device operating region beyond normal operation.

Thermal failure is one main reason to cause device failure under ESD stress conditions. A compact model is developed to predict the thermal failure with circuit simulators. Instead of analyzing the detailed failure mechanisms, a fixed failure temperature is introduced to indicate the device failure. The developed model can also address the thermal geometry with multiple stage structure.

P-N junction is the fundamental structure for most ESD protection devices, an enhanced diode model is proposed, including all physical effects when a diode is under ESD stress conditions, which are voltage overshoot, self heating effect, velocity saturation and thermal failure. By embedding a thermal failure monitor, the proposed model cannot only fit the I-V characteristics, but also predicts thermal failure for different pulses.

LDMOS transistors are widely used in power applications. Safe operating area (SOA) is an important factor to evaluate the LDMOS performance. A power defined transient SOA is modeled for short TLP stresses (<100ns). The device failure can be described with electronic thermal instability for short pulse stress and thermal electronic instability for long pulse stress.

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The public is welcome to attend.