Announcing the Final Examination of Faris Alghareb for the degree of Doctor of Philosophy

Time & Location: February 11, 2019 at 10:30 AM in HEC 356
Title: SOFT-ERROR RESILIENCE FRAMEWORK FOR RELIABLE AND ENERGY-EFFICIENT CMOS LOGIC AND SPINTRONIC MEMORY ARCHITECTURES

The revolution in chip manufacturing processes spanning five decades has proliferated high performance and energy-efficient nano-electronic devices across all aspects of daily life. In recent years, CMOS technology scaling has realized billions of transistors within large-scale VLSI chips to elevate performance. However, these advancements have also continually augmented the impact of Single-Event Transient (SET) and Single-Event Upset (SEU) occurrences which precipitate a range of Soft-Error (SE) dependability issues. Furthermore, the continuous shrinking of supply voltage reduces the required energy to induce transient and upset glitches at the susceptible nodes of a logic circuit. Consequently, SE mitigation techniques have become essential to improve systems' reliability. Herein, first, we proposed optimized soft-error resilience designs to improve robustness of sub-micron computing systems. The proposed approaches were developed to deliver energy-efficiency and tolerate double/multiple errors simultaneously while incurring acceptable speed performance degradation compared to the prior work.
Secondly, the necessity for energy-efficiency has given rise to run High Performance Computing (HPC) systems at Near-Threshold Voltage (NTV) region as opposed to the conventional approach of operating devices at nominal supply voltage. However, an increased Soft Error Rate (SER) has been identified as a significant concern for NTV operation of deeply-scaled CMOS logic paths. Thus, herein the impact of Process Variation (PV) at the NTV region on redundancy-based SE-mitigation approaches was investigated to highlight the approach that can realize favorable attributes, such as reduced critical datapath delay variation and low speed degradation. Finally, in recent years, spin-based devices have been widely used to design Non-Volatile (NV) elements such as NV latches and flip-flops, which can be leveraged in normally-off computing architectures for Internet-of-Things (IoT) and energy-harvesting-powered applications. Although spin-based devices can tolerate radiation particles, the corresponding CMOS circuitry required for their read/write operations is still susceptible to soft errors. Therefore, to make this emerging nanoscale device technology feasible, SE-tolerant approaches are presented herein to ensure the correct operation of hybrid CMOS/spin-based circuits in harsh environments. In the last portion of this dissertation, we design and evaluate for soft-error resilience NV latching circuits that can achieve intriguing features, such as low energy consumption, high computing performance, and superior soft errors tolerance, i.e., concurrently able to tolerate Multiple Node Upset (MNU), to potentially become a mainstream solution for the aerospace and avionic nanoelectronics. Together, these objectives cooperate to increase energy-efficiency and soft errors mitigation resiliency of larger-scale emerging NV latching circuits within iso-energy constraints.

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Approved for distribution by Ronald DeMara, Committee Chair, on January 25, 2019.
The public is welcome to attend.