GaN power devices are typically used in the 600 V market, for high efficiency, high power-density systems. For these devices, the lateral optimization of gate-to-drain, gate, and gate-to-source lengths, as well as gate field-plate length are critical for optimizing breakdown voltage and performance. This work presents a systematic study of lateral scaling optimization for high voltage devices to minimize figure of merit (RDS(on) x QG) and maximize breakdown voltage. In addition, this optimization is extended for low voltage devices (< 100 V), presenting results to optimize both lateral features and vertical features. For low voltage design, simulation work suggests that breakdown is more reliant on punch-through as the primary breakdown mechanism rather than on vertical leakage current as is the case with high-voltage devices.

A fabrication process flow has been developed for fabricating Schottky-gate, and MIS-HEMT structures at UCF in the CREOL cleanroom. The fabricated devices were designed to validate the simulation work for low voltage GaN devices. The UCF fabrication process is done with a four layer mask, and consists of mesa isolation, Ohmic recess etch, an optional gate insulator layer, ohmic metallization, and gate metallization. Following this work, the fabrication process was transferred to the National Nano Device Laboratories (NDL) in Hsinchu, Taiwan, to take advantage of the more advanced facilities there.

Following fabrication, a study has been performed on defect induced performance degradation, leading to the observation of a new phenomenon: trap induced negative differential conductance (NDC). Typically NDC is caused by self-heating, however by implementing a substrate bias test in conjunction with pulsed I-V testing, the NDC seen in our fabricated devices has been confirmed to be from buffer traps that are a result of poor channel carrier confinement during the dc operating condition.

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The public is welcome to attend.