Wide-bandgap Gallium Nitride (GaN) power devices provide inherent material advantages over silicon devices and have the potential to deliver superior performance for power electronics systems both in terms of power density and efficiency. As GaN-on-Si production scales to larger-diameter wafers, fabrication costs are continually reduced, making GaN integration even more desirable. Despite these advantages, GaN high electron mobility transistors (HEMTs) suffer from performance and reliability degradation as a result of trap centers within the device.

GaN power devices are typically used in the 600 V market, for high efficiency, high power-density systems. For these devices, the lateral optimization of gate-to-drain, gate, and gate-to-source lengths, as well as gate field-plate length are critical for optimizing breakdown voltage and performance. This work presents a systematic study of lateral scaling optimization for high voltage devices to minimize figure of merit ($R_{DS(on)} \times Q_G$) and maximize breakdown voltage. In addition, this optimization is extended for low voltage devices (< 100 V), presenting results to optimize both lateral features and vertical features. For low voltage design, simulation work suggests that breakdown is more reliant on punch-through as the primary breakdown mechanism rather than on vertical leakage current as is the case with high-voltage devices. Punch-through can be reduced by making the buffer more semi-insulating (by carbon doping). However, carbon doping has a negative impact on long-term reliability and leads to current collapse. This is seen in our measurement data as well, where GaN-on-Si devices grown with a graded buffer structure suffered from high stress, leading to high defect density in the buffer and poor passivation on the surface. This can cause trap induced negative differential conductance and can be mitigated by reducing growth stress, which can be done by using superlattice stress relief layers.

A fabrication process flow has been developed for fabricating Schottky-gate, and MIS-HEMT structures at UCF in the CREOL cleanroom. The fabricated devices were designed to validate the simulation work for low voltage GaN devices. The UCF fabrication process is done with a four layer mask, and consists of mesa isolation, Ohmic recess etch, an optional gate insulator layer.

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The public is welcome to attend.