Electrostatic discharge (ESD) is defined as the transfer of charge between objects at different potentials in a quite short time. Damages introduced by ESD events results in a loss of millions dollars to the semiconductor industry each year. ESD related failure is a major IC reliability concern and this is particularly true as microelectronics technology continues shrink to nanoâ€”metric dimensions. ESD design window research shows that ESD robustness of victim devices keep decreasing with technology scale. From 350nm bulk technology to 7nm FinFET technologies, ESD failure current ($I_{t2}$), ESD triggering voltage ($V_{t1}$) and gate break down voltage ($V_{gox}$) of victim Field Effect Transistors (FET) decrease a lot. In the meantime, parasitic capacitance of ESD diode with same $I_{t2}$ in FinFET technologies is ~3X compared with that in planar technologies. Thus transition from planar to FinFET technology requires more robust ESD protection however the large parasitic capacitance of ESD protection cell is problematic in highâ€”speed interface design.

To reduce the parasitic capacitance, a Dual Diode Silicon Controlled Rectifier (DDSCR) is presented in this dissertation. This design can exhibit high $I_{t2}$, small onâ€”state resistance ($R_{on}$), low overshoot voltage and low parasitic capacitance characteristics. Besides, different bounding materials lead to performance variations are compared. Millimeter wave technology is also demanded low capacitance ESD design. To address this consideration, a π filter like ESD network is presented, providing robust protection for 10â€”60 GHz RF circuit. Like a low pass π filter, it can reflect high frequency RF signals and transmit low frequency ESD pulses. Given proper inductor value, networks can work as robust ESD solutions at a certain Giga Hertz frequency range, making this design suitable for narrow band protection in millimeter wave I/Os.

To increase the holding voltage and reduce snapback, a resistor assist triggering heterogeneous stacking structure is discussed in this dissertation as a latchâ€”up free design, which can increase the holding voltage and also keep the trigger voltage nearly as same as a single SCR device.

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The public is welcome to attend.