Electrostatic discharge (ESD) is defined as the transfer of charge between objects at different potentials in a quite short time. Damages introduced by ESD events results in a loss of millions dollars to the semiconductor industry each year. ESD related failure is a major IC reliability concern and this is particularly true as microelectronics technology continues shrink to nano-meter dimensions.

ESD design window research shows that ESD robustness of victim devices keep decreasing with technology scale. From 350nm bulk technology to 7nm FinFET technologies, ESD failure current ($I_{t2}$), ESD triggering voltage ($V_{t1}$) and gate breakdown voltage ($V_{gox}$) of victim Field Effect Transistors (FET) decrease a lot. In the meantime, parasitic capacitance of ESD diode with same $I_{t2}$ in FinFET technologies is $\sim 3X$ compared with that in planar technologies. Thus transition from planar to FinFET technology requires more robust ESD protection however the large parasitic capacitance of ESD protection cell is problematic in high-speed interface design.

To reduce the parasitic capacitance, a Dual Diode Silicon Controlled Rectifier (DDSCR) is presented in this dissertation. This design can exhibit high $I_{t2}$, small on-state resistance ($R_{on}$), low overshoot voltage and low parasitic capacitance characteristics. Besides, different bounding materials lead to performance variations are compared.

Millimeter wave technology is also demanded low capacitance ESD design. To address this consideration, a $\pi$ filter like ESD network is presented, providing robust protection for 10–60 GHz RF circuit. Like a low pass $\pi$ filter, it can reflect high frequency RF signals and transmit low frequency ESD pulses. Given proper inductor value, networks can work as robust ESD solutions at a certain Giga Hertz frequency range, making this design suitable for narrow band protection in millimeter wave I/Os.

To increase the holding voltage and reduce snapback, a resistor assist triggering heterogeneous stacking structure is discussed in this dissertation as a latch-up free design, which can increase the holding voltage and also keep the trigger voltage nearly as same as a single SCR device.

Major: Electrical Engineering

Educational Career:
Bachelor’s of Microelectronics Technology, BS, 2013, University of Electronic Science and Technology of China
Master’s of Electrical Engineering, MS, 2016, University of Central Florida

Committee in Charge:
Kalpathy Sundaram, Chair, Electrical & Computer Engineering
Xun Gong, Electrical & Computer Engineering
Lei Wei, Electrical & Computer Engineering
Deliang Fan, Electrical & Computer Engineering
Javier Salcedo, Analog Device Inc.

Approved for distribution by Kalpathy Sundaram, Committee Chair, on May 31, 2018.

The public is welcome to attend.