To achieve efficiencies approaching the theoretical limit of 29.4% for industrially manufactured solar cells based on crystalline silicon, it is essential to have very low surface recombination velocities at both the front and rear surfaces of the silicon substrate. Typically, the substrate surfaces feature contacted and uncontacted regions, and recombination should be limited for both to maximize the energy conversion efficiency.

Uncontacted silicon surfaces are often passivated by the deposition of silicon nitride (SiNx) or an aluminum oxide film with SiNx as capping layer (Al2O3/SiNx stack). Further, proper surface preparation and cleaning of Si wafers prior to deposition also plays an important role in minimizing surface recombination. In the present work, the effect of various cleans based on different combinations of HCl, HF, HNO3, and ozonated deionized water (DIO3) on surface passivation quality of boronâ€”diffused and undiffused {100} nâ€”type Cz Si wafers was studied. It was observed that for SiNx passivated Si, carrier lifetime was strongly influenced by cleaning variations and that a DIO3â€”last treatment resulted in higher lifetimes. Moreover, DIO3+HF+HClâ†’HFâ†’DIO3 and HNO3â†’HFâ†’HNO3 cleans emerged as potential lowâ€”cost alternatives to HCl/HF clean in the photovoltaics industry.

Transmission electron microscopy (TEM) studies were carried out in order to get insight into the origin of variation in carrier lifetimes for different cleans. Changes in the surface cleans used were not found to have a significant impact on Al2O3/SiNx passivation stacks. However, an oxideâ€”last cleaning step prior to deposition of SiNx passivation layers was found to create a 1â€”2 nm SiOx tunnel layer resulting in excellent carrier lifetimes.

For contacted regions, low surface recombination can be achieved using passivated carrier selective contacts, which not only passivate the silicon surface and improve the open circuit voltage, but are also carrier selective. This means they only allow the majority carrier to be transported to the metal contacts, limiting recombination by reducing the number of minority carriers. Typically, carrier selectivity is achieved using a thin metal oxide layer, such as titanium oxide (TiO2) for electronâ€”selective contacts and molybdenum oxide (MoOx) for holeâ€”selective contacts. This is normally coupled with a very thin passivation layer (e.g., aâ€”Si:H, SiOx) between the silicon wafer and the contact.

In the present work, TiO2â€”based electronâ€”selective passivated rear contacts were investigated for nâ€”type câ€”Si solar cells. A low efficiency of 9.8% was obtained for cells featuring aâ€”Si:H/TiO2 rear contact, which can be attributed to rapid degradation of surface passivation of aâ€”Si:H upon FGA at 350Â°C due to hydrogen evolution leading to generation of defect states which increases recombination and hence a much lower Voc of 365 mV is obtained. On the other hand, 21.6% efficiency for cells featuring SiO2/TiO2 rear contact is due to excellent passivation of SiO2/TiO2 stack upon FGA anneal, which can be attributed to the presence of 1â€”2 nm SiO2 layer whose passivation performance improves upon FGA at 350Â°C whereas presence of large number of oxygen vacancies in TiO2â€”x reduces rear contact resistivity.

Likewise, MoOxâ€”based contacts were investigated as holeâ€”selective front contacts for an nâ€”type cell with a boronâ€”doped emitter. It has been previously reported that cell efficiencies up to 22.5% have been achieved with silicon heterojunction solar cells featuring a front contact wherein MoOx is inserted between aâ€”Si:H(i) and hydrogenated indium oxide (IO:H). However, device performance and FF in particular degrades upon annealing beyond 130Â°C. In this work, contact resistivity measurements by TLM technique in combination with TEM studies revealed that degradation of device performance is due to oxygen diffusion into MoOx upon annealing in air which reduces concentration of oxygen vacancies in MoOx and increases contact resistivity. The increase in contact resistivity reduces FF resulting in deterioration of device performance.