Time & Location: March 27, 2017 at 10:30 AM in HEC 356
Title: LDMOS Power Transistor Design and Evaluation using 2D and 3D Device Simulation

Power Semiconductor devices become increasingly important today due to strong demand of high energy-efficient power converters used for data centers, electrical vehicles, etc. In this thesis, the laterally double-diffused metal oxide semiconductor (LDMOS) power transistors suitable for highly integrated system on a chip (SOC) application has been studied.

Using the two-dimensional and three-dimensional Sentaurus device simulation, we examined different LDMOS structures to achieve enhanced figure of merit for low voltage (<30V) design. In Sentaurus device simulation, physical models such as doping and field-dependent mobility model, Okuto avalanche model, and Shockley-Read-Hall recombination model are accounted for. From our simulation results, the super-junction LDMOS offers a lower gate charge (QG) with a slightly increased specific on-resistance RDS(on) compared to those of a conventional LDMOS counterpart. The use of a floating P-layer design could reduce RDS(on) of the LDMOS. A lower RDS(on) is favorable to decrease the conduction loss of a power converter. In addition, the floating-P structure provides a simpler fabrication process and performance gain through device optimization. The implementation of shallow trench isolation (STI) help absorb the peak electric field at the gate edge. Combining the floating-P layer with a STI yields a much lower figure of merit, RDS(on)×QG = 5.93 mΩ-nC. According to our understanding that is the best figure of merit reported for 30V LDMOS design.

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Approved for distribution by Jiann-Shiun Yuan, Committee Chair, on March 10, 2017.

The public is welcome to attend.