In this dissertation paper, ESD models, especially ESD failure models for device thermal failure are introduced, with modeling methodology accordingly. First, an introduction for ESD event and typical ESD protection schemes are introduced. Its purpose is to give basic concept of ESD. Considering the universality of thermal failure in ESD device, it is imperative to establish a model to simulate ESD caused thermal failure.

Several works related to ESD model can be done. One crucial part for a failure model is to define the failure criterion. As common solution for ESD simulation and failure prediction. The maximum current level or breakdown voltage is used to judge whether a device fails under ESD stresses. Such failure criteria based on measurable voltage or current values are straightforward and can be easy to implement in simulation tools. However, the shortcoming of these failure criteria is each failure criterion is specifically designed for certain ESD stress condition. For example, the failure voltage levels for Human Body Model and Charged Device Model are quite different, and it is hard to judge a device’s ESD capability under standard test conditions based on its transmission line pulse test result. So it is necessary to look deeper into the physical mechanism of device failure under ESD and find a more universal failure criterion for various stress conditions.

As one of the major failure mechanisms, thermal failure evaluated by temperature is a more universal failure criterion for device failure under ESD stress. Whatever the stress model is, the device will fail if a critical temperature is reached at certain part inside the device and cause structural damage. Then finding out that critical temperature is crucial to define the failure point for device thermal failure. One chapter of this dissertation will focus on discussing this issue and propose a simple method to give close estimation of the real failure temperature for typical ESD devices.

Combined these related works, a comprehensive diode model for ESD simulation is proposed. Using existing ESD models, diode I-V characteristic from low current turn-on to high current saturation can be simulated. By using temperature as the failure criterion, the last point of diode operation, or the second breakdown point, can be accurately predicted.

Additional investigation of ESD capability of devices for special case like vertical GaN diode is discussed. Due to the distinct material property of GaN, the vertical GaN diode exhibits unique and interesting quasi-static I-V curves quite different from conventional silicon semiconductor devices. And that I-V curve varies with different pulse width, indicating strong conductivity modulation of diode neutral region that will delay the complete turn-on of the vertical GaN diode.

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The public is welcome to attend.