A new revolutionary concept was presented two decades ago, known as semiconductor Superjunction (SJ) theory to enhance the tradeoff relationship between specific on resistance $R_{sp}$ and offstate breakdown voltage $B_V$, in medium to high voltages (more than 100 V) power MOSFETs. The SJ concept was first applied and commercialized to vertical structures, but it hasn’t been used yet in low voltage MOSFETs with lateral structures. This thesis provides an investigation of the most common structures, principles and design techniques for discrete power MOSFETs. It also presents a simulation study of the application of these SJ concepts in the design of a Low Voltage SJ LDMOS transistor, using TCAD software. To make the device commercially feasible, this device design targets aggressive goals such as an off-state breakdown voltage of 60 V with $R_{sp}$ of 20 mΩ-mm$^2$. This study includes the analysis of the process flow for the fabrication of this transistor, using semiconductor technologies, and the simulation results, including Breakdown Voltage, on state resistance, electric field distribution among others simulation analysis.

Major: Electrical Engineering

Educational Career:
Bachelor’s of Electrical Engineering, BS, 2008, Universidad Autonoma de Manizales

Committee in Charge:
Jiann-Shiun Yuan, Chair, Electrical & Computer Engineering
Deliang Fan, Electrical & Computer Engineering
Kalpathy Sundaram, Electrical & Computer Engineering

Approved for distribution by Jiann-Shiun Yuan, Committee Chair, on June 7, 2016.

The public is welcome to attend.