Time & Location: July 6, 2016 at 10:00 AM in HEC 356
Title: Design and Optimization of Superjunction Vertical DMOS Power Transistors using Sentaurus Device Simulation

Vertical double-diffused metal oxide semiconductor (VDMOS) power transistor has been studied. The use of superjunction (SJ) in the drift region of VDMOS has been evaluated using three-dimensional device simulation. All relevant physical models in Sentaurus are turned on. The VDMOS device doping profile is obtained from process simulation. The superjunction VDMOS performance in off-state breakdown voltage and specific on-resistance is compared with that in conventional VDMOS structure. In addition, electrical parameters such as threshold voltage and gate charge are also examined. Increasing the superjunction doping in the drift region of VDMOS reduces the on-resistance by 26%, while maintaining the same breakdown voltage and threshold voltage compared to that of the conventional VDMOS power transistor with similar device design without using a superjunction.

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Approved for distribution by Jiann-Shiun Yuan, Committee Chair, on June 8, 2016.

The public is welcome to attend.