Scaling of semiconductors below nanometer range introduces serious design challenges that include high static power in memories and high leakage power, hindering further integration of CMOS devices. Thus, emerging devices are under intense analysis to overcome these drawbacks caused by transistor size scaling. Spintronics technology provides excellent features such as Non-Volatility, low read power, low read delay, higher scalability as well as easy integration with CMOS in comparison with SRAM memories. In addition, Carbon Nanotube Field Effect Transistors (CNFETs) provide superior electrical conductivity, low delay and low power consumption in comparison with conventional CMOS technology. Thus in this thesis, a unique approach to amalgamate spintronics memory technology with CNFET for logic drive in a reconfigurable computing architecture, to realizing ultimate circuit performance has been discussed.

A Carbon Magnetic Look-Up Table (CMâ€“LUT) is proposed, using a Magnetic Tunnel Junction (MTJ) spintronic device as memory element and CNFET to perform the logical operations to read the data stored in the aforementioned devices. The proposed circuit is radiation resilient, ultra-low power and high speed operation and the ability to withstand high temperature gradient, ideal for low power high performance battery operated mobile applications. In addition, the performance of hybrid drive for LUT to leverage fabrication feasibility of CMOS and performance of CNFET to realize fabrication cost effective design. The proposed 4â€“input 1â€“output CMâ€“LUT utilizes 41 CNFETs and 16 MTJs for read operation and 35 CNFETs to perform write operation. The results for CMâ€“LUT show 38 times energy reduction and 5.8 times faster circuit operation in comparison with CMOSâ€“based spinâ€“LUT.

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The public is welcome to attend.