Complementary metal oxide semiconductor (CMOS) radio frequency (RF) circuit design has been an ever-lasting research field. It has gained so much attention since RF circuits offer high mobility and wide-band efficiency, while CMOS technology provides the advantage of low cost and high integration capability. At the same time, CMOS device size continues to scale to the nanometer regime. Reliability issues with RF circuits have become more challenging than ever before. Reliability mechanisms, such as gate oxide breakdown, hot carrier injection, negative bias temperature instability, have been amplified as the device size shrinks. In addition, process variability becomes a new design paradigm in modern RF circuits.

In this Ph.D. work, a class F power amplifier (PA) was designed and analyzed using TSMC 180nm process technology. Its pre-layout and post-layout performances were compared. Post-layout parasitic effect decreases the output power and power-added efficiency. Physical insight of hot electron impact ionization and device self-heating was examined using the mixed-mode device and circuit simulation to mimic the circuit operating environment. Hot electron effect increases the threshold voltage and decreases the electron mobility of an n-channel transistor, which in turn decreases the output power and power-added efficiency of the power amplifier, as evidenced by the RF circuit simulation results. The device self-heating also reduces the output power and power-added efficiency of the PA. The process, voltage, and temperature (PVT) effects on a class AB power amplifier were studied. A PVT compensation technique using a current-source as an on-chip sensor was developed. The adaptive body bias design with the current sensing technique makes the output power and power-added efficiency much less sensitive to process variability, supply voltage variation, and temperature fluctuation, predicted by our derived analytical equations which are also verified by Agilent Advanced Design System (ADS) circuit simulation.

Process variations and hot electron reliability on the mixer performance were also evaluated using different process corner models. The conversion gain and noise figure were modeled using analytical equations, supported by ADS circuit simulation results. A process invariant current source circuit was developed to eliminate process variation effect on circuit performance. Our conversion gain, noise figure, and output power show robust performance against PVT variations compared to those of a traditional design without using the current sensor, as evidenced by Monte Carlo statistical simulation.

Finally, semiconductor process variations and hot electron reliability on the LC-voltage controlled oscillator (VCO) performance was evaluated using different process models. In our newly designed VCO, the phase noise and power consumptions are resilient against process variation effect due to the use of on-chip current sensing and compensation. Our Monte-Carlo simulation and analysis demonstrate that the standard deviation of phase noise in the new VCO design reduces about five times than that of the conventional design.

Major: Electrical Engineering

Educational Career:
Bachelor's of Electrical Engineering, BS, 2007, Kasetsart University
Master's of Electrical Engineering, MS, 2010, University of Central Florida

Committee in Charge:
Jiann S. Yuan, Chair, Electrical and Computer Engineering
Kalpathy B. Sundaram, Electrical and Computer Engineering
Lei Wei, Electrical and Computer Engineering
Mingjie Lin, Electrical and Computer Engineering
Lee Chow, Physics

Approved for distribution by Jiann S. Yuan, Committee Chair, on February 11, 2016.

The public is welcome to attend.