Time & Location: February 29, 2016 at 4:00 PM in HEC 450
Title: STUDY OF NOVEL POWER SEMICONDUCTOR DEVICES FOR PERFORMANCE AND RELIABILITY

For the purposes of this work, we focus primarily on the high voltage power semiconductor devices which are used in industrial power systems. A novel Trench Fast Recovery Diode (FRD) structure with injection control is proposed in this dissertation. The proposed structure achieves improved carrier profile without the need for excess lifetime control. This substantially improves the device performance, especially at extreme temperatures (−40 oC to 175 oC). The device maintains low leakage at high temperatures, and its Qrr and Irm do not degrade as is the usual case in heavily electron radiated devices. A 1600 diode using this structure has been developed, with a low forward turn-on voltage and good reverse recovery properties. The experimental results show that the structure maintains its performance at high temperatures.

In addition, we develop a termination scheme for the previously mentioned diode. A major limitation on the performance of high voltage power semiconductor is the edge termination of the device. It is critical to maintain the breakdown voltage of the device without compromising the reliability of the device by controlling the surface electric field. A good termination structure is critical to the reliability of the power semiconductor device. The proposed termination uses a novel trench MOS with buried guard ring structure to completely eliminate high surface electric field in the silicon region of the termination. The termination scheme was applied towards a 1350 V fast recovery diode, and showed excellent results. It achieved 98% of parallel plane breakdown voltage, with low leakage and no shifts after High Temperature Reverse Bias testing due to mobile ion contamination from packaging mold compound.

We also investigate the device physics behind a superjunction MOSFET structure for improved robustness. The biggest issue with a completely charge balanced MOSFET is decreased robustness in an Unclamped Inductive Switching (UIS) Circuit. The equally charged P and N pillars result in a flat electric field profile, with the peak carrier density closer to the P–N junction at the surface. This results in an almost negligible positive dynamic Rds(on) effect in the MOSFET. By changing the charge profile of the P–column, either by increasing it completely or by implementing a graded profile with the heavier P on top, we can change the field profile and the carrier density deeper into silicon, increasing the positive dynamic Rds(on) effect. Simulation and experimental results are presented to support the theory and understanding.

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Approved for distribution by Jiann S. Yuan, Committee Chair, on February 11, 2016.

The public is welcome to attend.