This PhD work investigates the impact of system-level type of ESD stress on components. Firstly, correlation factors between different ESD pulse types for different BEOL metal line topologies have been studied to support system level on-chip ESD design. The component level (HMM, HBM and TLP on wafer) and system level (IEC gun contact on package) ESD stresses were correlated followed by extraction of correlation factors between the IEC/HMM and TLP, as well as the HBM and TLP supported by analytical approximation. The major conclusions were verified using the thermal coupled mixed-mode simulations analysis. Secondly, operation of NLD MOS-SCR devices under the HMM and IEC air gap electrostatic discharge (ESD) stresses has been studied based on both the pulsed measurements and mixed-mode simulations. Under the IEC air gap testing, the devices are found to suffer the non-uniform multi-finger turn-on behavior and hence a relatively low passing level, while both the IEC contact and HMM stresses do not give rise to such an adversary effect and result in a considerably higher passing level. It is further shown that the non-uniform multi-finger turn-on effect depends on the stress pulse rise time. Such a dependency has also been examined and verified using the transmission line pulsing (TLP) technique with rise times ranging from 10 to 40ns.

In the last section, a new silicon-controlled rectifier (SCR) fabricated in a 30 V mixed-signal CDMOS (CMOS/DMOS) technology is presented. This device allows for robust EMI (electromagnetic interference) and ESD (electrostatic discharge) protection solution for high speed industrial interface applications operating in variable voltage swing range from -7V to +12V. This new SCR has reduced overshoot voltage and leakage current when electrically stressed under different pulse widths and temperatures. Analysis of the device physics is complemented via numerical TCAD mixed-mode simulations. A 200 x 200 µm² device designed in an annular configuration achieved > ± 8 kV IEC robustness by handling > ± 20 Amp of TLP current while clamping the voltage to ±3V within 2 ns.

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The public is welcome to attend.