Announcing the Final Examination of Vignesh Thangavel for the degree of Master of Science

Time & Location: April 7, 2015 at 3:00 PM in Harris Engineering Corporation (HEC) 450
Title: Cascaded Digital Refinement of Intrinsic Evolvable Hardware

Intrinsic evolution of reconfigurable hardware is sought to solve computational problems using the intrinsic processing behavior of System-on-Chip (SoC) platforms. SoC devices combine capabilities of analog and digital embedded components within a reconfigurable fabric under software control. A new technique is developed for these fabrics that leverages the digital resources' enhanced accuracy and signal refinement capability to improve circuit performance of the analog resources which are providing low power processing and high computation rates. In particular, Differential Digital Correction (DDC) is developed utilizing an error metric computed from the evolved analog circuit to reconfigure the digital fabric thereby enhancing precision of analog computations. The approach developed herein, Cascaded Digital Refinement (CaDR), explores a multi-level strategy of utilizing DDC for refining intrinsic evolution of analog computational circuits to construct building blocks, known as Constituent Functional Blocks (CFBs). They are developed in a cascaded sequence followed by digital evolution of higher-level control of these CFBs to build the final solution for the larger circuit at-hand. One such platform, Cypress PSoC-5LP was utilized to realize solutions to ordinary differential equations by first evolving various powers of the independent variable followed by that of their combinations to emulate mathematical series-based solutions for the desired range of values. This is shown to enhance accuracy and precision while incurring lower computational energy and time overheads.

Major: Electrical Engineering

Educational Career:
Bachelor's of Electrical and Electronics Engineering, BS, 2013, Birla institute of Technology and Sciences (BITS), Pilani
Master's of Electrical Engineering, MS, 2015, University of Central Florida

Committee in Charge:
Ronald F. DeMara, Chair, Department of Electrical engineering and Computer Science
Kalpathy B. Sundaram, Professor and Graduate Coordinator, Electrical and Computer Engineering Division, Department of Electrical engineering and Computer Science
Zixia Song, Associate Professor, Department of Mathematics

Approved for distribution by Ronald F. DeMara, Committee Chair, on March 13, 2015.

The public is welcome to attend.