Time & Location: March 2, 2015 at 12:00 PM in HEC 356  
Title: POST CONVERSION CORRECTION OF NON-LINEAR MISMATCHES FOR TIME INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS

Time Interleaved Analog-to-Digital Converters (TI-ADCs) utilize an architecture which enables conversion rates well beyond the capabilities of a single converter while preserving most or all of the other performance characteristics of the converters on which said architecture is based. Most of the approaches discussed here are independent of architecture; some solutions take advantage of specific architectures. Chapter 1 provides the problem formulation and reviews the errors found in ADCs as well as a brief literature review of available TI-ADC error correction solutions. Chapter 2 presents the methods and materials used in implementation as well as extend the state of the art for post conversion correction. Chapter 3 presents the simulation results of this work and Chapter 4 concludes the work. The contribution of this research is three fold: A new behavioral model was developed in Simulink and MATLAB to model and test linear and nonlinear mismatch errors emulating the performance data of actual converters. The details of this model are presented as well as the results of cumulant statistical calculations of the mismatch errors which is followed by the detailed explanation and performance evaluation of the extension developed in this research effort. Leading post conversion correction methods are presented and an extension with derivations is proposed. It is shown that the data converter subsystem architecture developed is capable of realizing better performance compared with those currently reported in the literature while having a more efficient implementation.

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Approved for distribution by Wasfy Mikhael, Committee Chair, on February 10, 2015.

The public is welcome to attend.