Evaluating the use of Silicon-Controlled Rectifiers (SCRs) for Electrostatic Discharge (ESD) protection, this dissertation explores the layout factors and design mechanisms affecting SCR's ESD performance, including trigger voltage, holding voltage, robustness, and turn-on speed. Three innovative designs are proposed based on traditional SCR and using advanced and commercial technologies, with assistance from TCAD simulations and wafer experiments. For low-voltage CMOS technologies, a novel design of PMOS-triggered bidirectional SCR achieves low trigger voltage and improved turn-on speed, while a direct-connected SCR is proposed and verified with no snapback behavior and outstanding turn-on performance for single-direction protection. For high-voltage BCD technology, the structure of high-voltage SCR is improved to exhibit no snapback and high holding voltage, while maintaining high robustness. Finally, an ESD protection circuit using pHEMT is proposed for the emerging GaN technology.