Electrostatic Discharge (ESD) has been reported to be in charge of more than 35% of failure in integrated circuits (ICs). Generally, ESD protections are evaluated after wafer and/or system fabrication, increasing the development period and cost if the protections cannot meet customer’s requirements. Therefore, it is important to design and customize robust and area-efficient ESD protections for the ICs at the development stage. Silicon-controlled rectifier (SCR) has become a promising candidate for ESD protection purpose, thanks to its high robustness, high area efficiency, and flexibility for modification to meet different protection requirements.

In this dissertation, the layout factors and important design mechanisms are evaluated on SCR’s ESD performance, including trigger voltage, holding voltage, robustness, and turn-on speed. Three innovative designs are proposed based on traditional SCR and used different advanced and commercial technologies, with assistance from TCAD simulation and wafer experiments. For low-voltage CMOS technologies, a novel design of PMOS-triggered bidirectional SCR successfully achieves low trigger voltage and improved turn-on speed, while a direct-connected SCR is proposed and verified with no-snapback behavior and outstanding turn-on performance for dual- and single-direction protection respectively. For high-voltage BCD technology, the structure of high-voltage SCR is improved to exhibit no snapback and high holding voltage, and simultaneously maintain high robustness. Finally, an ESD protection circuit using pHEMT is proposed for the first time for the emerging GaN technology.

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The public is welcome to attend.