Electrostatic Discharges (ESD) is a significant hazard to electronic components and systems. Based on a specific process technology, a given circuit application requires a customized ESD consideration that meets all the requirements such as the device's operating voltage, leakage current, breakdown constrains and sizes. As new technology nodes mature every 3-5 years, design of effective ESD protection solution has become more and more challenging due to the narrowed design window, elevated electric field and current density. The ESD related failure is a major IC reliability concern and results in a loss of millions dollars each year in the semiconductor industry.

Increasingly stringent design specifications are forcing original equipment manufacturers (OEMs) requires a high level of ESD robustness and the integrated circuit (IC) level, while finding ways to streamline the ESD characterization during early development cycle. New the human metal model (HMM) test model has been introduced. With the investigation of the first research work, we have developed a new characterization methodology, providing more accurate and consistent results.

The design and analysis of the ESD protection devices itself has also been shown in this research work. A new dual-polarity SCR optimized for high bidirectional blocking voltages, high trigger current and low capacitance is realized in a sub 3-V, 180-nm CMOS process. This ESD device is designed for a specific application where the operating voltage at the I/O is larger than that of the core circuit. Then, we have looked into the ESD protection designs in the 28-nm CMOS technology. An ESD protection design builds on the multiple discharge-paths ESD cell concept and focuses the attention on the detailed design, optimization and realization of the in-situ ESD protection cell for IO pins with variable operation voltages. By introducing different device configurations fabricated in a 28-nm CMOS process, a greater flexibility in the design options and design trade-offs can be obtained in the proposed topology, thus achieving a higher integration and smaller cell size definition for multi-voltage compatibility interface ESD protection applications. Also the performance of the ESD device under different environmental situation (variable temperature) has been also investigated.

Major: Electrical Engineering

Educational Career:
Bachelor’s of Microelectronics, BS, 2010, Chongqing University of Posts and Telecommunications
Master’s of Electrical Engineering, MS, 2012, University of Central Florida

Committee in Charge:
Juin J. Liou, Chair, EECS
Jiann-Shiun Yuan, UCF
Xun Gong, EECS
Yier Jin, EECS
Javier Salcedo, Analog Devices Inc.

Approved for distribution by Juin J. Liou, Committee Chair, on January 16, 2015.

The public is welcome to attend.