The scaling of semiconductor transistors has led to a decrease in thickness of the silicon dioxide layer used as gate dielectric. The thickness of the silicon dioxide layer is reduced to increase the gate capacitance, thus increasing the drain current. If the thickness of the gate dielectric decreases below 2nm, the leakage current due to the tunneling increases drastically. Hence, it is necessary to replace the gate dielectric, silicon dioxide, with a physically thicker oxide layer of high-k materials like Hafnium oxide and Titanium oxide. High-k dielectric materials allow the capacitance to increase without a huge leakage current.

Hafnium oxide and Titanium oxide films are deposited by reactive magnetron sputtering from Hafnium and Titanium targets respectively. These oxide layers are used to create metal-insulator-metal (MIM) structures using aluminum as the top and bottom electrodes. The films are deposited at various O2/Ar gas flow ratios, substrate temperatures, and process pressures. After attaining an exact recipe for these oxide layers that exhibit the desired parameters, MOS capacitors are fabricated with n-Si and p-Si substrates having aluminum electrodes at the top and bottom of each. Comparing the parameters of Hafnium oxide- and Titanium oxide-based MOS capacitors, MOSFET devices are designed with Hafnium oxide as gate dielectric.

Major: Electrical Engineering

Educational Career:
Bachelor’s of Electronics Engineering, BS, 2011, Vishwakarma Institute of Information Technology, Pune

Committee in Charge:
Kalpathy Sundaram, Chair, Electrical Engineering and Computer Science
Vikram Kapoor, Electrical Engineering and Computer Science
Parveen F. Wahid, Electrical Engineering and Computer Science

Approved for distribution by Kalpathy Sundaram, Committee Chair, on January 1, 2014.

The public is welcome to attend.