Future microprocessors pose many design challenges to the voltage regulators and power conversion techniques. Multiphase synchronous buck converters have been widely used in high current low voltage microprocessor application. Design optimization needs to be carefully carried out to meet the stringent specification and power saving features. The primary focus and objective of this work is to comprehensively investigate the current and voltage dynamics of the multiphase synchronous buck converter. We focus on optimizing the topology to achieve optimal efficiency and highest possible reliability based on the real system running conditions and corner case scenarios.

We first start with the efficiency optimization from static operation and present load adaptive control. With better understanding of the power loss in several modes of operation, i.e. buck, PFM and boost modes, which cover all the operation scenarios of CPU VR. Driver interface is thoroughly investigated here for operation and efficiency purposes. An efficiency optimization routine is generated by parametric variation.

We propose the load transient enhancement schemes to minimize the output voltage excursion during low repetitive load transient. We first study the DCR current sense impact for the AVP loop, which can effectively shape the output voltage excursion. During load engage, the pulses should be pulled in fast enough to compensate the voltage deviation. During load release, adaptive body braking schemes are proposed to adaptively suppress the voltage overshoot during load release. Special design consideration needs to be carried out during slow phase shedding that the inductor current in the shedded phase needs to be ramped down to zero before turn OFF the phase. During system wake-up operation, a corner case operation is captured and new dead-time management scheme is proposed to maintain the high efficiency while ensure the system reliability.

In the high repetitive rate of load transient, we first study the sampling nature of PWM converter. The small signal closed loop system output impedance is derived and the PID values are optimised in the high frequency range to attenuate the high frequency system noise. Beat frequency is studied and mitigated by proposing load frequency detection scheme by turning OFF the nonlinear loop and introducing current protection in the control loop.

Multiphase converter design capable of dynamic voltage scaling (DVS) is presented in at last. Modes of operation are thoroughly studied first. Optimized driver dead-time in boost mode operation are illustrated in order to achieve dynamic voltage regulation during dynamic VID (DVID) operation. The excessive stress on the control MOSFET which increases the reliability concern is captured in boost mode operation. Feasible solutions are also proposed and verified by both simulation and experiment results. \( \text{CdV/dt} \) compensation for removing the AVP effect and novel nonlinear control scheme for smooth transition are proposed for dealing with fast voltage positioning. Optimum phase number control during dynamic voltage transition is also proposed and triggered by voltage identification (VID) delta to further reduce the dynamic loss.

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The public is welcome to attend.