Electrostatic Discharge (ESD) phenomenon is a common phenomenon in daily life and it could damage the integrated circuit throughout the whole cycle of product from the manufacturing. Several ESD stress models and test methods have been used to reproduce ESD events and characterize ESD protection device’s performance. The basic ESD stress models are: Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM). On-chip ESD protection devices are widely used to discharge ESD current and limit the overstress voltage under different ESD events. Some effective ESD protection devices reported for low speed circuit applications such as analog ICs or digital ICs in CMOS process. On the contrast, only a few ESD protection devices available for radio frequency integrated circuits (RF ICs). The ESD protection for RF ICs in GaAs pHEMT process is very difficult, and the typical HBM protection level is below 1-kV HBM level. The first part of our work is to analyze pHEMT’s snapback, post-snapback saturation and thermal failure under ESD stress using TLP-like Sentaurus TCAD simulation. The snapback is caused by virtual bipolar transistor due to large electron-hole pairs impacted near drain region. Post-snapback saturation is caused by temperature-induced mobility degradation due to III-V compound semiconductor materials’ poor thermal conductivity. And thermal failure is found to be caused by hot spot located in pHEMT’s InGaAs layer. Several novel ESD protection devices were designed in 0.5um GaAs pHEMT process. The multi-gate pHEMT based ESD protection devices in both enhancement-mode and depletion-mode were reported and characterized then. Due to the multiple current paths available in the multi-gate pHEMT, the new ESD protection clamp showed significantly improved ESD performances over the conventional single-gate pHEMT ESD clamp, including higher current discharge capability, lower on-state resistance, and smaller voltage transient. Then we optimized SiGe-based silicon controlled rectifiers (SiGe SCR) in SiGe BiCMOS process. SiGe SCR is considered a good candidate ESD protection device in this process. But the possible slow turn-on issue under CDM ESD events is the major concern. In order to optimize the turn-on performance of SiGe SCR against CDM ESD, the Barth 4012 very fast TLP (vFTLP) and vFTLP-like TCAD simulation were used for characterization and analysis. It was demonstrated that a SiGe SCR implemented with a P PLUG layer and minimal PNP base width can supply the smallest peak voltage and fastest response time which is resulted from the fact that the impact ionization region and effective base width in the SiGe SCR were reduced due to the presence of the P PLUG layer. In the end, we optimized SCRs in standard silicon-based CMOS process to supply protection for high speed/radio-frequency ICs. SCR is again considered the best for its excellent current handling ability. But the parasitic capacitance of SCRs needs to be reduced to limit SCR’s impact to RF performance. We proposed a novel SCR-based ESD structure and characterize it experimentally for the design of effective ESD protection in high-frequency CMOS based integrated circuits.

Major: Semiconductor Devices and Reliability

Educational Career:
Bachelor’s of Semiconductor Devices and Reliability, BS, 2006, Zhejiang University
Master’s of Semiconductor Devices and Reliability, MS, 2008, Zhejiang University

Committee in Charge:
Dr. Juin J. Liou, Chair, Electrical Engineering and Computer Science
Dennis Deppe, College of Optics & Photonics
John Z. Shen, Electrical Engineering and Computer Science
Jiann S. Yuan, Electrical Engineering and Computer Science
Thomas Wu, Electrical Engineering and Computer Science
Michael G. Haralambous, Electrical Engineering and Computer Science
Approved for distribution by Dr. Juin J. Liou, Committee Chair, on December 20, 2012.

The public is welcome to attend.