Electrostatic Discharge (ESD) is one of the most prevalent threats to electronic components. Every technology or each circuit application requires a custom ESD consideration that includes the devices’ footprint, leakage current, operating voltage, and gate oxide breakdown voltage. The goal of this research is to develop novel, effective and robust ESD protection solutions for emerging technologies and modern CMOS technologies.

Silicon nanowire transistors and organic thin film transistors have been deemed as promising alternative CMOS technologies in the beyond Moore Era, yet their ESD performances have not been investigated in previous literatures. In this work, the dimension parameters, fabrication process, biasing conditions, and layout dependency of such devices under Human Body Mode ESD stresses are studied experimentally in company with failure analysis revealing the failure mechanism induced by ESD. The findings, including extracted figure of merit, design window and methodologies, and failure mechanism, should provide useful insight into the development of ESD protection solutions for the next-generation nanowire and organic based integrated circuits.

Based on modern technologies, research endeavor has been placed in the design and analysis of a major ESD protection device: diode-triggered-silicon-controlled-rectifier (DTSCR). First, a new type of DTSCR having bi-directional conduction capability, optimized design window, high HBM robustness and low parasitic capacitance are developed. Second, the Human Body Mode and Charged Device Mode ESD robustness of DTSCRs using four typical layout topologies are explored, and layouts offering best overall performance are proposed.

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The public is welcome to attend.