CMOS RF circuit design has been an ever-lasting research field. It gained so much attention since RF circuits have high mobility and wide band efficiency, while CMOS technology has the advantage of low cost and high integration capability. At the same time, CMOS device size continues to scale down to the nanometer regimes. Reliability issues with RF circuits have become more challenging than ever before. Reliability effects, such as gate oxide breakdown, hot carrier injection, negative bias temperature instability, have been amplified as the device size shrinks. In addition, process variability becomes a new design issue in RF circuits.

In this work, a class E power amplifier (PA) is designed and fabricated using TSMC 0.18 µm RF technology. Oxide stress and hot electron experiments were carried out at increased supply voltage. Power amplifier performance before and after RF stress were measured and compared. Mixed mode device and circuit simulation results provided physical insights to support experimental data. It is proved that hot carrier effects degrade PA performances such as output power and power added efficiency. Temperature and self-heating effects on a class AB power amplifier were examined. Different gate biasing techniques were analyzed and their abilities to compensate output power were compared. A simple gate biasing circuit to compensate the PA temperature variations has been proposed. This adaptive gate biasing scheme can effectively reduce the effect of temperature variations on the PA over a wide range of temperatures.

Process variation effects on a Colpitts oscillator using Monte-Carlo simulation were studied. Phase noise was modeled using analytical equations, supported by ADS simulation results. An adaptive body biasing circuit was proposed to eliminate process variation. Simulation results from probability density function demonstrated its capability to relieve process variation effects on phase noise. Standard deviation of phase noise with adaptive body bias is much less than that without using any compensation.

Finally, a robust, adaptive design technique using phase lock loop (PLL) as an on-chip sensor to reduce Process, Voltage, Temperature (PVT) variations and other aging effects on RF PA was evaluated. The frequency and phase of ring oscillator in PLL intend to change after PVT variations. However, the control signal to the ring oscillator provides a compensation effect to keep the frequency of ring oscillator unchanged. Therefore, the control voltage implicitly accounts for PVT and aging effects. This control signal is converted to adaptive body bias to stabilize the power amplifier output power. ADS simulation results demonstrate that the adaptive body bias using on-chip sensing control signal is sufficient to provide output power stability over PVT variations and aging effects, indicated by analytical equations.

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The public is welcome to attend.