A methodology to obtain design guidelines for gate oxide input pin protection and high voltage output pin protection in Electrostatic Discharge (ESD) time frame is developed through measurements and Technology Computer Aided Design (TCAD).

A set of parameters based on transient measurements are used to define Transient Safe Operating Area (TSOA). The parameters are then used to assess effectiveness of protection devices for output and input pins. The methodology for input pins includes establishing ESD design targets under Charged Device Model (CDM) type stress in low voltage MOS inputs.

The methodology for output pins includes defining ESD design targets under Human Metal Model (HMM) type stress in high voltage Laterally Diffused MOS (LDMOS) outputs. First, the assessment of standalone LDMOS robustness is performed, followed by establishment of protection design guidelines. Secondly, standalone clamp HMM robustness is evaluated and a prediction methodology for HMM type stress is developed based on standardized testing. Finally, LDMOS and protection clamp parallel protection conditions are identified.

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The public is welcome to attend.