The underlying physical mechanisms of destructive single event effects (SEE) from heavy ion radiation have been widely studied in traditional vertical double-diffused power MOSFETs (VDMOS). Recently, lateral double-diffused power MOSFETs (LDMOS), which inherently provide lower gate charge than VDMOS, have become an attractive option for MHz-frequency DC-DC converters in terrestrial power electronics applications. There are growing interests in extending the LDMOS concept into radiation-hard space applications. Since the LDMOS has a device structure considerably different from VDMOS, the well-studied single event burn-out (SEB) or single event gate rapture (SEGR) response of VDMOS cannot be simply assumed for LDMOS devices without further investigation.

A few recent studies have begun to investigate ionizing radiation effects in LDMOS devices, however, these studies were mainly focused on displacement damage and total ionizing dose (TID) effects, with very limited data reported on the heavy ion SEE response of these devices. Furthermore, the breakdown voltage of the LDMOS devices in these studies was limited to less than 80 volts (mostly in the range of 20-30 volts), considerably below the voltage requirement for some space power applications.

In this work, we numerically and experimentally investigate the physical insights of SEE in two different fabricated LDMOS devices designed by the author and intended for use in radiation hard applications. The first device is a 24 V Resurf LDMOS fabricated on P-type epitaxial silicon on a P+ silicon substrate. The second device is a much different 150 V SOI Resurf LDMOS fabricated on a 1.0 micron thick N-type silicon-on-insulator substrate with a 1.0 micron thick buried silicon dioxide layer on an N-type silicon handle wafer. Each device contains internal features, layout techniques, and process methods designed to improve single event and total ionizing dose radiation hardness. Technology computer aided design (TCAD) software was used to develop the transistor design and fabrication process of each device and also to simulate the device response to heavy ion radiation. Using these simulations in conjunction with experimentally gathered heavy ion radiation test data, we explain and illustrate the fundamental physical mechanisms by which destructive single event effects occur in these LDMOS devices. We also explore the design tradeoffs for making an LDMOS device resistant to destructive single event effects, both in terms of electrical performance and impact on other radiation hardness metrics.

Major: Electrical Engineering

Educational Career:
Bachelor’s of Electrical Engineering, BS, 2006, UCF
Master’s of Electrical Engineering, MS, 2007, UCF

Committee in Charge:
Prof. Zheng Shen, Chair, EECS
Prof. Jiann-Shiunn Yuan, EECS
Prof. Kalpathy Sundaram, EECS
David Okada, PhD, Great Wall Semiconductor, Inc.

Approved for distribution by Prof. Zheng Shen, Committee Chair, on October 18, 2011.

The public is welcome to attend.