DRAMs represent the main memory at which data is stored. It is organized in Ranks, Banks, Rows and Columns, in which the smallest storage element is represented by the transistor-capacitor pair, and addressed according to its location in the DRAM hierarchy.

Lowest-level cache misses are satisfied by the main memory by mapping the cache-line physical address to the corresponding set of memory cells that contain the data. This is done by identifying the rank, bank, row and column to start fetching the data from in bursts. The address mapping can happen through a specific devised scheme in the memory controller, that receives the request from the CPU, decodes the address to locate the data, and responds accordingly.

Though multiple schemes can be used to map the cache-line physical address to the proper location of the data, only one is used and hard-coded in the memory controller. Our investigation showed that applications’ performance varies according to the mapping scheme used.

Up to the date of this research, no previous work was done to investigate the usage of a dynamic address mapping schemes to provide higher performance and lower power consumption by utilizing memory level parallelism. We propose a simple thread-aware memory controller design that provides dynamic mapping scheme to different threads. Results showed that the proposed design achieves better performance and power efficiency compared to the single-static scheme used.

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The public is welcome to attend.