This study investigated the Class F and inverse Class F RF power amplifier operating at 5.8 GHz. The breakdown voltage of CMOS power transistor is the major challenging issue in design and implementation of high power RF power amplifiers especially in sub-micron CMOS technology. In order to alleviate this problem, cascode topologies were implemented to reduce the Drain-to-Source voltage (stress). A Cascode Class F & Inverse Class F RF power amplifier were designed, and optimized in order to improve efficiency and reliability using 0.18μm CMOS technology process. A 50% decrease in the stress has been achieved in the cascode class-F and Inverse class F amplifiers.

The sensitivity and temperature effect were investigated using BSIM-4 model. Such an amplifier was designed and optimized for a good sensitivity. A substrate bias circuit was implemented to achieve a good sensitivity. Recommendations for future advancements were made for modification and optimization of the circuit by the application of other stress reduction strategies, variation in the class-F and inverse class F topology, and improvement of the substrate bias circuit.

Major: Electrical Engineering

Educational Career:
Bachelor's of Electronics and Communication Engineering, BS, 2000, University of Madras

Committee in Charge:
Dr. Jiann S. Yuan, Chair, Electrical Engineering and Computer Science
Dr. Kalpathy B. Sundaram, Electrical Engineering and Computer Science
Dr. Lee Chow, College of Science, Physics

Approved for distribution by Dr. Jiann S. Yuan, Committee Chair, on June 21, 2011.

The public is welcome to attend.