Dr. Mark Heinrich

School of EECS
4000 Central Florida Boulevard
University of Central Florida
Orlando, FL 32816-2362

Office: (407) 882-0138
Fax: (407) 823-5419
http://www.cs.ucf.edu/~heinrich/
heinrich@eecs.ucf.edu

Education:

Ph.D. 1998 Stanford University, *Electrical Engineering*
The Performance and Scalability of Distributed Shared Memory Cache Coherence Protocols
Advisor: John Hennessy

M.S. 1993 Stanford University, *Electrical Engineering*

B.S.E. 1991 Duke University, *Double Major: Electrical Engineering/Computer Science*
GPA: 3.98/4.0, First in Class

Research Interests:

Parallel computer architecture; mobile and low-power architectures, active memory and I/O systems, scalable distributed shared-memory cache coherence protocols; hardware/software co-design; scalable web services

Professional Experience:

2002– **Associate Professor** **University of Central Florida**
School of EECS
Served as Chair of Computer Science Department, April-September 2005, then as Associate Director of the combined School of EECS, 2005-2007.

2004- **Founder, Chief Technical Officer** **Phanfare, Inc.**
Online photo and video hosting company. Responsible for deploying scalable web service supported by web, iPhone, Mac, and PC clients as well as for the system architecture, and managing relationships with DataPipe managed hosting and Amazon Web Services.

1998–2002 **Assistant Professor, ECE** **Cornell University**
Member, Graduate Fields of Electrical and Computer Engineering and Computer Science. Co-founder, Computer Systems Laboratory.

1998 **Teaching Fellow** **Stanford University**
Co-taught EE 182 (Computer Organization) with John Hennessy.

1997–2000 **Founder, Chief Scientist** **Flashbase, Inc.**
Database-backed web forms and sweepstakes engine. Helped raise $1MM in venture capital from Dawntreader, a division of Wit Capital. 7 full-time employees with office in Manhattan. Acquired by DoubleClick Inc. in May 2000.

1992–1998 **Research Assistant** **Stanford University**
Prof. John L. Hennessy, Computer Systems Laboratory.
Scalable distributed shared-memory multiprocessors; architecture and implementation of the Stanford FLASH multiprocessor; design and evaluation of scalable cache coherence protocols; developed first model for evaluating the effect of node controller occupancy in distributed shared-memory machines; wrote FlashLite, the multi-threaded system simulator for the FLASH project.

1994– **Independent Engineering Consultant**

Air Force Research Labs: active memory systems; DoubleClick Inc.: research and development and technical due-diligence for business development; Xerox PARC: implementation and synthesis of an ATM switch; Talkway, Inc.: Java programming for an Internet startup; Silicon Graphics: parallel computer architecture; Heller, Ehrman, White & McAufliffe and Hickman, Beyer & Weaver LLP: patent law consulting.

Honors, Awards, and Memberships:

ACM SIGARCH and IEEE-CS TCCA ISCA Influential Paper Award, 2009

IBM Faculty Award, 2004–2005

Cornell University College of Engineering's Michael Tien '72 Excellence in Teaching Award, Spring 2001

NSF CAREER Award, 2000–2004, "Flexible Architectures for Data-Intensive Computing"

Cornell University IEEE Teacher of the Year Award, 1999–2000

"The Stanford FLASH Multiprocessor" selected as one of best papers in 25 years of ISCA

National Science Foundation Graduate Fellow, 1991–1994

Graduated 1st in class, Duke University, Summa Cum Laude

IBM Thomas J. Watson Scholarship, 1987–1991

General Motors Scholarship, 1989–1990

Phi Beta Kappa

Tau Beta Pi

Eta Kappa Nu

Senior Member IEEE, IEEE Computer Society

Member: Association for Computing Machinery

Professional Activities:

Workshops Chair, International Symposium on High-Performance Computer Architecure (*HPCA*) Salt Lake City, Utah, February 2008. Sponsors: IEEE Computer Society

Architecture Area Program Committee, International Conference for High-Performance Computing and Communications (*SC07*), Reno, NV, November 2007. Sponsors: IEEE Computer Society, ACM

Program Committee, International Parallel and Distributed Processing Symposium (*IPDPS*), Long Beach, CA, March 2007. Sponsors: IEEE Computer Society, ACM

Program Committee, International Conference on Parallel Processing (*ICPP*), Columbus, OH, August 2006. Sponsors: IEEE Computer Society

Program Committee, International Conference on Parallel and Distributed Systems (*ICPADS*), Minneapolis, MN, July 2006. Sponsors: IEEE Computer Society

Program Committee, Second Workshop on Advanced Networking and Communications Hardware (ANCHOR), International Symposium on Computer Architecture (*ISCA*), Madison, Wisconsin, June 2005. Sponsors: IEEE Computer Society, ACM

NSF Panelist: CAREER Program. Director: Peter Varman. Washington, D.C., December 2004

Program Committee, First Workshop on Advanced Networking and Communications Hardware (ANCHOR), International Symposium on Computer Architecture (*ISCA*), Munich, Germany, June 2004. Sponsors: IEEE Computer Society, ACM

Program Committee, Fourth Workshop on Communication Architecture for Clusters (CAC '04), International Parallel and Distributed Processing Symposium (*IPDPS*), Santa Fe, New Mexico, April 2004. Sponsors: IEEE Computer Society, ACM

Program Committee, Third Workshop on System Area Networks (SAN-3), International Symposium on High-Performance Computer Architecure (*HPCA*) Madrid, Spain, February 2004. Sponsors: IEEE Computer Society

Program Committee and Workshop Chair, Tenth International Conference on High-Performance Computer Architecture (*HPCA*), Madrid, Spain, February 2004. Sponsors: IEEE Computer Society

Program Committee, International Conference on Parallel Processing (*ICPP*), Taiwan, October 2003. Sponsors: International Association for Computers and Communications

NSF Panelist: Computer Systems Architecture. Director: Peter Varman. Washington, D.C., May 2003

Program Committee, Seventeenth International Parallel and Distributed Processing Symposium (*IPDPS*), Nice, France, April 2003. Sponsors: IEEE Computer Society, ACM

Program Committee, Third Workshop on Communication Architecture for Clusters (CAC '03), International Parallel and Distributed Processing Symposium (*IPDPS*), Nice, France, April 2003. Sponsors: IEEE Computer Society, ACM

NSF Panelist: ITR Program. Director: Peter Varman. Washington, D.C., February 2003

Program Chair and Organizer, Second Workshop on Novel Uses of System Area Networks (SAN-2), International Symposium on High-Performance Computer Architecure (*HPCA*) Anaheim, CA, February 2003. Sponsors: IEEE Computer Society

Program Committee & Session Chair, Sixteenth International Parallel and Distributed Processing Symposium (*IPDPS*), Ft. Lauderdale, FL, April 2002. Sponsors: IEEE Computer Society, ACM

Selected Invitee, First Annual DARPA/NRL/USSOCOM Conference for Scientists Helping America, Washington, D.C., March 2002

Program Chair and Organizer, First Workshop on Novel Uses of System Area Networks (SAN-1), International Symposium on High-Performance Computer Architecure (*HPCA*) Boston, MA, February 2002. Sponsors: IEEE Computer Society

Invited Panelist, NSF Workshop on Computer Performance Evaluation. Austin, TX, December 2001

Program Committee, Tenth International Conference on Parallel Architectures and Compilation Techniques (*PACT*), Barcelona, Spain, September 2001. Sponsors: IEEE, ACM

Program Committee, Workshop on Caching, Coherence, and Consistency (*WC3*), ACM Conference on Supercomputing, Sorrento, Italy, June 2001. Sponsors: ACM

Panelist, Mathematics, Information, and Computational Sciences Division within the Office of Advanced Scientific Computing Research in the Office of Science at the U.S. Department of Energy (*DOE*), April 2001

Publicity Chair, Seventh International Symposium on High-Performance Computer Architecture (*HPCA*), Monterrey, Mexico, January 2001. Sponsor: IEEE Computer Society

Participant: Design Automation Conference (*DAC*) (1998); Hot Chips (1993–1997); Hot Interconnects (August 1993); HPCA Workshop on Novel Uses of System Area Networks (*SAN*) (2002-04); International Conference on Distributed Processing Techniques and Applications (*PDPTA*) (2002); International Parallel and Distributed Processing Symposium (*IPDPS*) (2002); International Symposium on Architectural Support for Programming Languages and Operating Systems (*ASPLOS*) (1994–2002); International Symposium on High-Performance Computer Architecture (*HPCA*) (2004); International Symposium on Computer Architecture (*ISCA*) (1993–1994, 1998–2006); ISCA Shared Memory Workshop (1994, 1998–2000); ISCA Workshop on Solving the Memory Wall (2000); International Symposium on High-Performance Computing (*ISHPC*) (2002); International Symposium on Microarchitecture (*MICRO*) (2001); Symposium on the Principles and Practice of Parallel Programming (*PPOPP*) (1993); Scientists Helping America (2002)

Referee: ACM International Conference on Measurement and Modeling of Computer Systems (*SIGMETRICS*); ACM SIGPLAN Conference on Programming Language Design and Implementation (*PLDI*); ACM Transactions on Architecture and Code Optimization (*TACO*); ACM Transactions on Computer Systems (*TOCS*); European Conference on Parallel Computing; Hawaii International Conference on System Sciences; Hot Interconnects; IEEE Computer; IEEE Computer Architecture Letters (*CAL*); IEEE Transactions on Computers (*TOC*); IEEE Transactions on Parallel and Distributed Systems (*TPDS*); International Conference on Parallel Architectures and Compilation Techniques (*PACT*); International Conference on Parallel Processing (*ICPP*); International Conference on Supercomputing (*ICS*); International Journal of Parallel and Distributed Systems and Networks; International Parallel Processing Symposium (*IPPS*); International Parallel and Distributed Processing Symposium (*IPDPS*); International Symposium on Architectural Support for Programming Languages and Operating Systems (*ASPLOS*); International Symposium on Computer Architecture (*ISCA*); International Symposium on High-Performance Computer Architecture (*HPCA*); International Symposium on Microarchitecture (*MICRO*); Journal of Parallel and Distributed Computing (*JPDC*); Journal of Systems and Software; Proceedings of the IEEE; Symposium on Parallel Algorithms and Architectures (*SPAA*); Symposium on the Principles and Practice of Parallel Programming (*PPOPP*)

Distinguished Lectures and Conference Presentations:

"Exploiting Active CMP-based Devices in System Area Networks." Third Workshop on System Area Networks (SAN-3), Madrid, Spain, February 2004.

"Single-node and Multi-node Active Memory Systems." Seminar, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, February 2003.

"Cache Coherence Protocol Design for Active Memory Systems." International Conference on Parallel and Distributed Processing Techniques and Applications, Las Vegas, NV, June 2002.

"Active Memory Clusters: Efficient Multiprocessing on Commodity Clusters." International Symposium on High-Performance Computing, Kansai Science City, Japan, May 2002.

"Active Memory Clusters: Efficient Multiprocessing on Commodity Clusters." Seminar, School of Electrical Engineering and Computer Science, University of Central Florida, Orlando, FL, April 2002.

"Active Memory Systems: A Unified Uniprocessor and Multiprocessor Approach." Seminar, IBM Austin Research Labs, Austin, TX, December 2001.

"Active Memory Systems Research." Seminar, IBM Research, Yorktown, NY, September 2001.

"Active Memory Clusters." Seminar, Intel Corporation, Hillsboro, OR, August 2001.

"Active Memory Clusters: Efficient Multiprocessing on Next-Generation Servers." Processor and Platform Research Forum, Intel Corporation, Santa Clara, CA, August 2001.

"Flash Forward: Better, Faster, Cooler," Cornell University Silicon Valley Event, hosted by Hunter Rawlings, San Mateo, CA, April 2001.

"Providing Hardware DSM Performance at Software DSM Cost." Seminar, University of Rochester, April 2001.

"Hardware DSM Performance at Software DSM Cost," Air Force Research Laboratory, Rome, NY, March 2001.

"Simulation vs. Reality: The Importance of Building Hardware," CS Colloquium, Cornell University, February 2001.

"A Case for Asynchronous Active Memories," ISCA Workshop on Solving the Memory Wall, Vancouver, Canada, June 2000.

"Data-Intensive Computing," Lockheed Martin Federal Systems Seminar, Owego, NY, June 1999.

Invited speaker at Stanford Engineering School reception for John Hennessy becoming Provost of Stanford University. Speakers: Condoleezza Rice, Mark Horowitz, and Mark Heinrich. June 2, 1999.

"The Performance and Scalability of Distributed Shared Memory Cache Coherence Protocols," Seminar, School of Electrical Engineering, Cornell University; CS Department, SUNY Stonybrook; CS Department, University of Virginia; CS Department, University of Pennsylvania; CS Department, Duke University; CS Department, Rutgers University; March 1998. CS Department, University of Texas; ECE Department, Carnegie Mellon University; April 1998.

"Coherence Protocols and the Impact of Flexibility," IBM T.J. Watson Research Seminar, Yorktown, NY, January 1995.

"The Performance Impact of Flexibility in the Stanford FLASH Multiprocessor," International Symposium on Architectural Support for Programming Languages and Operating Systems, October, 1994.

"FLASH Architecture and Status," ISCA Shared Memory Workshop, Chicago, IL, April, 1994.

University Activities:

Chair, EECS Diversity Hiring Committee, UCF, 2011

Chair, EECS Faculty Recruiting Committee, UCF, 9/2005–07, 2009–10

Member, CECS Diversity Committee, UCF, 2008–present

Member, EECS Strategic Planning Committee, UCF, 2009–10

Associate Director, School of EECS, UCF, 9/2005–5/2007

Chair, EECS Undergraduate Curriculum Reform Committee, UCF, 9/2005–2007

Member, EECS ABET Committee, UCF, 2006–2007

Member, I2Lab Steering Committee, UCF, 2005–2007

Member, CECS Sabbatical Committee, UCF, 2007

Member, CECS Human Resources Director Search, UCF, 2006, 2010–11

Member, UCF Assistant Director of Development Search, UCF, 2006

Member, DARPA Urban Challenge Team, UCF, 2006–2007

Interim Director, School of Computer Science, UCF, 4/2005–9/2005

Member, CS Faculty Recruiting Committee, UCF, 2003–2004

Member, CS Director Chair Recruiting Committee, UCF, 2003–2004

Member, CS Tenure/Promotion Review Committee, UCF, 2004–2005

Member, CS Yet Another (Budget) Committee, UCF, 2003–2004

Alternate Member, CS Tenure/Promotion Review Committee, UCF, 2003–2004

Member, CECS RIA Awards Committee, UCF, 2004–2005

Member, Intelligent Information Systems Institute, Cornell University, March 2001–2002

Member, College of Engineering Teaching Awards Committee, Cornell, 2002

Member, ECE Experimental Systems Search Committee, Cornell, 2000–2002

Member, ECE Curriculum & Standards Committee, Cornell, 2000–2002

Member, ECE Computer Advisory Committee, Cornell, 1999–2002

Member, ECE Long-Range Recruiting Committee, Cornell, 1999–2002

Member, ECE Circuits & MEMS Search Committee, Cornell, 1999–2001

Member, ECE Computer Systems Search Committee, Cornell, 1998–2000

Committee Member, CURIE Summer Program for Women in Engineering 1999–2002

Webmaster, CURIE Summer Program for Women in Engineering 2000–2002

Project Coordinator, CURIE Summer Program for Women in Engineering 2002

Project: Privacy, Security, and Functionality: Designing Boundaries in the Digital World

Panelist, New Faculty Orientation, September, 2000

Panelist, Engineering College Council, Cornell, October, 2000

Co-founder, Computer Systems Laboratory, October 1998

Teaching Experience:

2003– **Associate Professor** **University of Central Florida**

Spring 2011:
Computer Organization (CDA 3103), 75 students
Parallel Computer Architecture (CDA 6107), 17 students

Fall 2010:
Computer Architecture (EEL 4768), 61 students, *SPI 4.6071*
Advanced Computer Architecture (CDA 5106), 33 students *SPI 4.5833*

Spring 2010:
Advanced Computer Architecture (CDA 5106), 24 students *SPI 4.5000*

Fall 2009:
Computer Architecture (EEL 4768), 80 students
Advanced Computer Architecture (CDA 5106), 46 students *SPI 4.6000*

Spring 2007:
Computer Architecture (CDA 4150), 45 students

Spring 2006:
Parallel Computer Architecture (CDA 6107), 12 students

Spring 2005:
Parallel Computer Architecture (CDA 6107), 13 students

Fall 2004:
Computer Architecture (CDA 4150), 34 students

Spring 2004:
Parallel Computer Architecture (CDA 6107), 33 students

Fall 2003:
Computer Architecture (CDA 4150), 56 students

1998-2003 **Assistant Professor** **Cornell University**

Fall 2002:
Parallel Computer Architecture (ECE 572), 53 students

Spring 2002:
Computer Organization (ECE/CS 314), 313 students

Fall 2001:
Parallel Computer Architecture (ECE 572), 36 students
Topics in Computer Systems (ECE 697), 27 students

Spring 2001:
Parallel Computer Architecture (ECE 572), 45 students

Fall 2000:
Computer Architecture (ECE 475), 75 students

Spring 2000:
Parallel Computer Architecture (ECE 572), 32 students
Plus in Computer Organization (ECE/CS 314), 205 students
Developed & Taught: Topics in Computer Systems (future ECE 697), 15 students

Fall 1999:
Developed & Taught: Computer Architecture (ECE 475), 102 students

Spring 1999:
Developed & Taught: Parallel Computer Architecture (ECE 572), 45 students
Plus in Fundamentals of Computer Engineering (ECE 308), ∼80 students

Fall 1998:
Plus in Microprocessor Architectures (ECE 475), 85 students

2000-01 **Field Lecturer** **CURIE Program, Cornell University**
Gave ECE Field Session lecture and lab for the CURIE Summer Program for Women in Engineering, as well as talks on ECE for prospective engineering Freshmen women.

1998 **Teaching Fellow** **Stanford University**
Co-taught Computer Organization (EE 182) with John Hennessy, ∼175 students.

1996 **Independent Tutor** **Heller, Ehrman, White & McAufliffe**
Gave lectures on basic Computer Systems concepts to patent attorneys.

Advising:

Current Graduate Student Advisees:

Jacob Staples (MS. UCF, CpE); *Expected graduation: Summer 2011*
Research Topic: Single-chip Smartphones

Rami Jadaa (MS. UCF, EE); *Expected graduation: Summer 2011*
Research Topic: Power Efficiency in Multicore Smartphones

Current Undergraduate Research Advisees:

Former Graduate Student Advisees:

Anton Kiriwas (MS. UCF, CS); *Graduated: December 2006*
Thesis: Scalable Multithreaded Computing

Mainak Chaudhuri (Ph.D. Cornell University, ECE); *Graduated: May 2004*
Thesis: Architectural Extensions for Executing Coherence Protocol Threads on Multi-threaded Microprocessors with Integrated Memory Controllers

Daehyun Kim (Ph.D. Cornell University, ECE); *Graduated: August 2003*
Thesis: Architectural Support for Cache-coherent Active Memory Systems

Jesse Chang (M.Eng., ECE); *Graduated: August 2002*
Thesis: IA-64 Processor Simulation Techniques

Benjamin Hertzberg (M.Eng., ECE); *Graduated: August 2002*
Thesis: Branch Processor: Compiler/Architecture Interactions

Jennifer Lee (M.Eng., ECE); *Graduated: August 2002*
Thesis: MIPS R10000 Processor Simulator

Yang Lin (M.Eng., ECE); *Graduated: August 2002*
Thesis: IA-64 Processor Simulation Techniques

Derrin Berger (M.Eng., ECE); *Graduated: May 2002*
Thesis: Implementing Active Memory Systems in FPGAs

Stephen Enochson (M.Eng., CS); *Graduated: May 2002*
Thesis: Modeling Active Memory Elements

Jeremy Schreiber (M.Eng., ECE); *Graduated: December 2001*
Thesis: Software Simulation of a 64-bit Itanium Processor

David Chen (M.Eng., EE); *Graduated: May 2001*
Thesis: Out-of-order Processor Simulation Techniques

Brian Morgan (M.Eng., CS); *Graduated: December 2000*
Thesis: A Verilog to CAST Synthesizer

Brandon Backlund (M.Eng., EE); *Graduated: August 2000*
Thesis: Cache Coherence Protocol Design

Ji Bae (M.Eng., EE); *Graduated: May 2000*
Thesis: Operating Systems for Active I/O Architectures

Binson Wei (M.Eng., EE); *Graduated: May 2000*
Thesis: Operating Systems for Active I/O Architectures

Joe Lee (M.Eng., CS); *Graduated: December 1999*
Thesis: Programming Environment for Active I/O Systems

Former Undergraduate Research Advisees:

Alva Bandy (CS); *Graduated: May 2004*
Research Topic: Porting PLI code to VCS for CDA 4150

Ethan Bancala (CS); *Graduated: May 2004*
Research Topic: Superscalar Processor Scheduling

Zennard Sun (ECE); *Graduated: May 2004*
Research Topic: Superscalar Processor Scheduling

Chris Foster (ECE); *Graduated: May 2002*
Research Topic: Modeling Modern Memory Systems

Oscar Ramirez (ECE); *Graduated: May 2002*
Research Topic: Parallelizing and Optimizing Code for Multiprocessor Systems

Dawn Lee (ECE); *Graduated: May 2001*
Research Topic: Applications for Active I/O Systems

Larry Pellach (ECE); *Graduated: May 2001*
Research Topic: Serial to JTAG Conversion for Multiprocessor Consoles

Jeremy Kowalczyk (ECE); *Graduated: May 2000*
Research Topic: Active I/O Systems

Avichai Lissack (CS); *Graduated: May 2000*
Research Topic: Active I/O Systems

Fayaz Onn (ECE); *Graduated: May 2000*
Research Topic: SCSI systems for Active I/O Architectures

Tom Chi (ECE); *Graduated: May 1999*
Research Topic: Applications for Active I/O Systems

Paul Coleman (CS); *Graduated: May 1999*
Research Topic: Exceptions, Interrupts, and Context-Switching on the MIPS R3000

Eric Twardzicki (ECE); *Graduated: May 1999*
Research Topic: Applications for Active I/O Systems

PUBLICATIONS

* *denotes student author, AR % denotes conference acceptance rate, GSC denotes Google Scholar citations as of 2010.*

Total number of Google Scholar citations: 1669

Journals:

Under Review/In Preparation: N/A

Accepted, To Appear: N/A

Accepted, In Print:

M. Chaudhuri and M. Heinrich. Integrated Memory Controllers with Parallel Coherence Streams. *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, **18**(8):1159-1173, August 2007.

M. Chaudhuri* and M. Heinrich. Exploring Virtual Network Selection Algorithms in DSM Cache Coherence Protocols. *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, **15**(8):699-712, August 2004.

D. Kim*, M. Chaudhuri*, M. Heinrich, and E. Speight. Architectural Support for Uniprocessor and Multiprocessor Active Memory Systems. *IEEE Transactions on Computers*, **53**(3):288-307, March 2004. *GSC: 15*

M. Chaudhuri* and M. Heinrich. The Impact of Negative Acknowledgments in Scalable Shared-Memory Multiprocessors. *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, **15**(2):134-150, February 2004. *GSC: 12*

M. Chaudhuri*, M. Heinrich, C. Holt, et al. The Effects of Latency, Occupancy, and Bandwidth in DSM Multiprocessors: Simulation, Modeling, and Experimental Results. *IEEE Transactions on Computers*, **52**(7):862–880, July 2003. *GSC: 15*

J. Hennessy, A. Gupta, and M. Heinrich. Cache-Coherent Distributed Shared Memory: Perspectives on Its Development and Future Challenges. *Proceedings of the IEEE*, **87**(3):418–429, Special Issue on Distributed Shared Memory, March 1999. *GSC: 38*

M. Heinrich et al. A Quantitative Analysis of the Performance and Scalability of Distributed Shared Memory Cache Coherence Protocols. *IEEE Transactions on Computers*, **48**(2):205–217, Special Issue on Cache Memory and Related Problems, February 1999. *GSC: 18*

M. Heinrich et al. Hardware/Software Codesign of the Stanford FLASH Multiprocessor. In *Proceedings of the IEEE*, **85**(3), Special Issue on Hardware/Software Co-design, March 1997. *GSC: 15*

Refereed Conferences:

Under Review/In Preparation: N/A

Accepted, To Appear: N/A

Accepted, In Print:

D. D. Kalamkar, M. Chaudhuri, and M. Heinrich. Simplifying Active Memory Clusters by Leveraging Directory Protocol Threads. *In IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2007.

M. Chaudhuri* and M. Heinrich. SMTp: An Architecture for Next-generation Scalable Multi-threading. In *Proceedings of the 31st International Symposium on Computer Architecture (ISCA)*, pages 124–135, June 2004. *AR: 14% GSC: 19*

M. Hao* and M. Heinrich. Exploiting Active CMP-based Devices in System Area Networks. *In the 3rd Workshop on System Area Networks (SAN-3) held in conjunction with HPCA*, February 2004. *GSC: 1*

M. Heinrich and M. Chaudhuri*. Ocean Warning: Avoid Drowning. *Computer Architecture News*, **31**(3):30-32, June 2003. *GSC: 6*

D. Kim*, M. Chaudhuri*, and M. Heinrich. Active Memory Techniques for ccNUMA Multiprocessors. In *Proceedings of the 17th International Parallel and Distributed Processing Symposium (IPDPS)*, April 2003. *AR: 29% GSC: 5*

M. Hao* and M. Heinrich. Active I/O Switches in System Area Networks. In *Proceedings of the 9th International Symposium on High-Performance Computer Architecture (HPCA)*, pages 365–376, February 2003. *AR: 21% GSC: 2*

D. Kim*, M. Chaudhuri*, and M. Heinrich. Leveraging Cache Coherence in Active Memory Systems. In *Proceedings of the 16h International Conference on Supercomputing (ICS)*, pages 2–13, June 2002. (*Daehyun Kim: Winner, Best Student Presentation*) *AR: 21% GSC: 27*

M. Chaudhuri*, D. Kim*, and M. Heinrich. Cache Coherence Protocol Design for Active Memory Systems. In *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA)*, pages 83–89, June 2002. *GSC: 22*

M. Heinrich, E. Speight, and M. Chaudhuri*. Active Memory Clusters: Efficient Multiprocessing on Commodity Clusters. In *Proceedings of the Fourth International Symposium on High Performance Computing (ISHPC), Lecture Notes in Computer Science vol. 2327*, Springer-Verlag, pages 78–92, May 2002. *AR: 31% GSC: 8*

J. Gibson, R. Kunz, D. Ofelt, M. Horowitz, J. Hennessy, and M. Heinrich. FLASH vs. (Simulated) FLASH: Closing the Simulation Loop. In *Proceedings of the 9th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 49–58, November 2000. *AR: 21% GSC: 112*

A. Chou, B. Chelf, D. Engler, and M. Heinrich. Using Meta-Level Compilation to Check FLASH Protocol Code. In *Proceedings of the 9th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 59–70, November 2000. *AR: 21% GSC: 23*

R. Manohar and M. Heinrich. A Case for Asynchronous Active Memories. In *Proceedings of the ISCA Workshop on Solving the Memory Wall*, (10 pages), June 2000. *GSC: 10*

J. Kuskin, D. Ofelt, M. Heinrich, et al. The Stanford FLASH Multiprocessor. Reprinted in *Selected Papers from 25 Years of ISCA*, pages 485–496, August 1998. *GSC: 54*

R. Soundararajan, M. Heinrich, B. Verghese, et al. Flexible Use of Memory for Replication/Migration in Cache-Coherent DSM Multiprocessors. In *Proceedings of the 25th International Symposium on Computer Architecture (ISCA)*, pages 342–355, June 1998. *AR: 21% GSC: 56*

K. Olukotun, M. Heinrich, and D. Ofelt. Digital System Simulation: Methodologies and Examples. In *Proceedings of the 35th Design Automation Conference (DAC)*, pages 658–663, June 1998. *GSC: 28*

M. Martonosi, D. Ofelt, and M. Heinrich. Integrating Performance Monitoring and Communication in Parallel Computers. In *ACM SIGMETRICS International Conference on Measurement and Modeling of Computer Systems*, pages 138–147, May 1996. *AR: 21% GSC: 55*

J. Hennessy and M. Heinrich. Hardware/Software Co-Design of Processors: Concepts and Examples. In *Hardware/Software Co-design*, edited by G. de Micheli and M. Sami, Kluwer Academic Publishers, 1996. *GSC: 18*

M. Heinrich et al. The Performance Impact of Flexibility in the Stanford FLASH Multiprocessor. In *Proceedings of the 6th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 274–285, 1994. *AR: 19% GSC: 158*

J. Kuskin, D. Ofelt, M. Heinrich, et al. The Stanford FLASH Multiprocessor. In *Proceedings of the 21st International Symposium on Computer Architecture (ISCA)*, pages 302–313, April 1994. *AR: 23% GSC: 828*

Ph.D. Dissertation:

M. Heinrich. The Performance and Scalability of Distributed Shared Memory Cache Coherence Protocols. Ph.D. Dissertation, Stanford University, October 1998. *GSC: 23*

Technical Reports:

M. Heinrich and E. Speight. Active Memory Clusters: Efficient Multiprocessing on Next-Generation Servers. Cornell CSL Technical Report CSL-TR-2001-1014, August 2001.

B. Morgan and M. Heinrich. V2CAST: A Synthesis Tool. Cornell Computer Systems Technical Report CSL-TR-2000-1009, December 2000.

M. Heinrich and E. Speight. Providing Hardware DSM Performance at Software DSM Cost. Cornell Computer Systems Technical Report CSL-TR-2000-1008, November 2000. *GSC: 6*

J. Gibson, R. Kunz, D. Ofelt, and M. Heinrich. A Study in the Accuracy of Architectural Simulation. Cornell Computer Systems Technical Report CSL-TR-2000-1004, June 2000.

R. Manohar and M. Heinrich. The Branch Processor Architecture. Cornell Computer Systems Technical Report CSL-TR-1999-1000, November 1999. *GSC: 2*

R. Manohar and M. Heinrich. ActiveRAM: An Architecture for Programmable, High-Performance Memory Systems. Cornell Computer Systems Technical Report CSL-TR-1998-991, October 1998.

M. Heinrich and R. Manohar. Active Fabric: An Architecture for Programmable, Scalable I/O Subsystems. Cornell Computer Systems Technical Report CSL-TR-1998-990, October 1998.

C. Holt, M. Heinrich, J. P. Singh, et al. The Effects of Latency, Occupancy, and Bandwidth in Distributed Shared Memory Multiprocessors. Technical Report CSL-TR-95-660, Computer Systems Laboratory, Stanford University, January 1995. *GSC: 87*

FUNDING

Pending Proposals:

None.

Funded Proposals:

1. *Scalable Multi-threaded Multiprocessor Architectures*. Funded by IBM Faculty Awards Program. PI: Mark Heinrich. IBM Contact: Evan Speight. 2004–2005. $40,000.
2. *CAREER: Flexible Architectures for Data-Intensive Computing.* Funded by the National Science Foundation, transfer to University of Central Florida. PI: M. Heinrich. Feb 2004–Feb 2005. $80,946.
3. *CAREER: Flexible Architectures for Data-Intensive Computing.* Funded by the National Science Foundation. PI: M. Heinrich. June 1, 2000–May 31, 2004. $257,675 + $10,000 University Unrestricted Fund + $10,000 Engineering College Match.
4. *Active Fabric I/O Systems.* Funded by Altera Corporation PI: M. Heinrich. October 1999. No Expiration. $20,000.
5. *Data-Intensive Computing.* Funded by Lockheed Martin Federal Systems. PI: M. Heinrich. December 31, 1998–August 31, 2000. $25,000.

Equipment Grants:

1. *Intel Itanium IA-64 Server.* Donated by Intel. M. Heinrich and E. Speight. October 2001. $25,000.
2. *32-node IBM SP-2 Multiprocessor.* Donated by the Theory Center. M. Heinrich and E. Speight. February 2001. $1,000,000.
3. *Logic Analyzers.* Donated by Tektronix. M. Heinrich and R. Manohar. August 1999. $75,000.
4. *Intel Computer Systems Teaching Lab.* Donated by Intel. M. Heinrich and R. Manohar. August 1999. $319,495.
5. *Software For Computer Systems Teaching Lab.* Donated by Microsoft. M. Heinrich and R. Manohar. August 1999. $116,955.
6. *High-Speed Initiative Equipment Match.* Donated by Hewlett-Packard. R. D'Andrea, J. Belina, M. Heinrich, E. Kan, P. Krusius, P. Kintner. August 1999. $244,997.
7. *High-Speed Initiative.* Donated by Robert Tishman. R. D'Andrea, J. Belina, M. Heinrich, E. Kan, P. Krusius, P. Kintner. August 1999. $300,000.

Additional Student Funding:

1. *Intelligent Information Systems Institute.* 1 Ph.D. student. M. Heinrich. AY 2001–2002 and AY 2002-2003.
2. *Intelligent Information Systems Institute.* 2 Ph.D. students. M. Heinrich. Summer 2001 and Summer 2002.

Total Funding Generated From All Sources (excluding pending): $2,429,122.